NEXSYS® Component Technology

NEXSYS® Components

For VIVISUN Advanced Lighted Pushbutton Switches and Indicators, NEXSYS Modules, and NEXSYS Thru-Hole Devices (THD).

ARINC 429 Signal Converters

Defined Logic

Solid State Relay

Electronic Latch

Electronic Rotary

Pulse/Timer

Time Delay

Square Wave Oscillator

Voltage Sensor

Current Sensor

Diode Pack

Terminal Block

NEXSYS® Module and Configurations

VIVISUN® Body Configurations

NEXSYS® Thru-Hole Devices

Document Type	Technical Guide
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Document Overview

The purpose of this document is to provide complete technical information on NEXSYS components, NEXSYS Module, internal component configurations, and NEXSYS Thru-Hole Devices manufactured by Applied Avionics.

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- Email: **support@appliedavionics.com**, or
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Document Revision History (last 5 revisions shown)			
Revision	**Effective Date**	**Approved By**	**Description**
--	02/01/2022	LKJ	Initial Release
A	04/23/2024	LKJ	Added MPTB data, SSR3 Data, On-State Resistance Operating Parameter updates on ARINC Converters, DL, SSR, EL, ER, SWO. VS, and CS, Propagation Input Timing Operating Parameter update on DL, added RF Conducted Susceptibility Electrical Qualifications for SSR3, changed 22-006 to 22-026, added /116, /117 info
B	09/10/2024	MH	Corrected Category for Electrostatic Discharge row in Appendix A Table A.2
C	10/08/2024	KL	Removed Parity paragraph from Section 2.1.1, added more Power Input Aircraft Power qualifications to table A.2 Electrical Qualifications

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1.0 NEXSYS® Component Technology – Overview

NEXSYS Component Technology is a platform of solid-state and discrete electronic components used to create custom multi-function digital and analog control circuits. The form factor of NEXSYS® Components allows them to be packaged inside VIVISUN switch and indicator bodies; see Section 4.0, inside NEXSYS Modules; see Section 3.0, or as a Thru-Hole Device; see Section 5.0. NEXSYS components can function independently or in combination with other NEXSYS components, electromechanical switches, and aircraft systems.

Applied Avionics has a dedicated NEXSYS Application Development Team to assist with design and implementation. NEXSYS application engineers can develop wiring diagrams, LTSpice® simulations, configure part numbers and help with troubleshooting. For questions and application assistance, contact a NEXSYS application engineer at 1-888-848-4786.

The Applied Avionics Part Configurator (https://configurator.appliedavionics.com/) makes it easy to configure a complete solution using NEXSYS Component Technology, including ready-to-order part numbers and specification of:

- VIVISUN Switches and Indicators
- NEXSYS Component Options
- NEXSYS Modules and Thru-Hole Devices
- NEXSYS and VIVISUN Accessories (i.e., Connector Plug, Mounting Hardware)

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2.0 NEXSYS® Components

NEXSYS components are solid-state devices that contain no firmware or software and are designed, tested, and qualified to perform reliably in the most demanding military and commercial applications. NEXSYS components are packaged inside VIVISUN switches and indicators (Compact and High Capacity), NEXSYS Modules, and are available as Thru-Hole Devices. For specific performance characteristics, each NEXSYS component section includes parametric data.

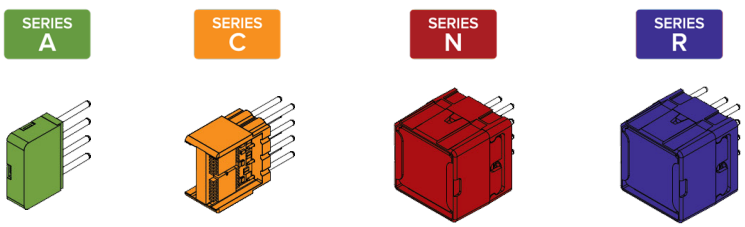
Component Performance

The NEXSYS Components are commercial-off-the-shelf (COTS) items. This standard catalog hardware includes features to allow for flexible interface design solutions while also meeting aircraft performance standards. The NEXSYS Components are designed, tested, and qualified to MIL-PRF-22885/116, MIL-PRF-22885/117, DO-160 and MIL-STD-461 requirements. Specifications are available in our MIL-PRF and DO-160 Documents page, and the qualification table is available in Appendix A. Detailed test data is made available upon request.

Component Series

Four (4) component series designations define the form factor and number of I/O pins: Series A, Series C, Series N, or Series R, see Figure 2.0.0.0-A. Component series also refers to functionality, configuration, and packaging options of NEXSYS components.

Figure 2.0.0.0-A



Component Configurations

NEXSYS components are packaged inside VIVISUN switches and indicators (Compact and High Capacity), NEXSYS Modules, and are available as Thru-Hole Devices, see Figure 2.0.0.0-B.

- For NEXSYS Module packaging options, see Section 3.0.
- For VIVISUN switch and indicator packaging options, see Section 4.0.
- For NEXSYS Thru-Hole Device specifications, see Section 5.0.

Figure 2.0.0.0-B

	NEXSYS Module (See 3.1)	**VIVISUN Compact Body** (See 4.1.1)	**VIVISUN High Capacity Body** (See 4.1.2)	**NEXSYS Thru-Hole Devices** (See 5.1)
SERIES A	✓	✓	✓	✓
SERIES C	✓		✓	✓
SERIES N	✓		✓	✓
SERIES R	✓		✓	✓

Component Functions and Series

NEXSYS Components are categorized according to application function, and summarized in the table below.

Figure 2.0.0.0-C		
Function	**Description**	**Series**
Data Conversion		
ARINC 429 Signal Converters	Autonomous ARINC 429 receivers with the protocol logic necessary to capture and convert a specified data-word to discrete output(s), controlled by the decode of a single label and bit, multiple-bits, or multi-bit Binary Decode (BD), see 2.1.1.	SERIES N SERIES R
Signal Switching/Control		
Defined Logic	Digital electronic device that performs Boolean logic gate operations *AND*, *OR*, *NOT*, *NAND*, *NOR*, *XOR*, *XNOR*, as well as *BUFFER*, see 2.2.1.	SERIES C
Solid State Relay	Normally Open (NO) and Normally Closed (NC) solid-state relays available individually (SSR) or in a combination of four (SSRCH). The bidirectional inputs are polarity insensitive, and the device performs buffered switching with optical isolation between inputs and outputs, see 2.2.2.	SERIES A SERIES C
State Control		
Electronic Latch	Electronic latching with multiple trigger modes to activate orthogonal switching (flip-flop) between two known states and a 1Hz blink output, see 2.3.1.	SERIES C
Electronic Rotary	Electronic rotary control that performs incremental switching through a loop of up to four latched output states, controlled by input level transitions, see 2.3.2.	SERIES C
Timing		
Pulse/Timer	Dual-channel edge detector and pulse generator with independent channels to perform stable retriggerable/resettable one-shot operation for fixed timing applications. Pulse-width output timing options range from 125 ms to 20 sec, see 2.4.1.	SERIES C
Time Delay	Time-delay output, controlled by input triggers or power-up. Output timing options range from 125 ms to 4 hrs, see 2.4.2.	SERIES A
Square Wave Oscillator	Oscillating output controlled by input triggers or power-up. Frequency (cycles/sec) and Period (sec/cycle) options range from 0.25 Hz (4 sec) to 500 Hz (0.002 sec), see 2.4.3.	SERIES A
Sensing		
Voltage Sensor	Direct Current (DC) voltage sensor performs undervoltage and overvoltage detection to trigger the output. Sensed-voltage (VSD1) setpoint options range from +1 to 48 VDC, and sensed-low voltage (VSD2) setpoint options range from 50 mVDC to 1000 mVDC (+1 VDC), see 2.5.1.	SERIES A
Current Sensor	Direct Current (DC), low-side current sensor that performs undercurrent and overcurrent detection to trigger the output. Sensed-current setpoint options range from 10 mA to 1000 mA (1.0 A), see 2.5.2.	SERIES A
Passive		
Diode Pack	Package of two diodes specified as either commercial (1N6484) or military (1N5621JANTX) grade, see 2.6.1.	SERIES A
Terminal Block	4-splice configuration for increased wiring efficiency, see 2.6.2.	SERIES A

2.1 Data Conversion Components

Components that interface with system serial buses and convert data from one format to another.

Data Conversion components include:

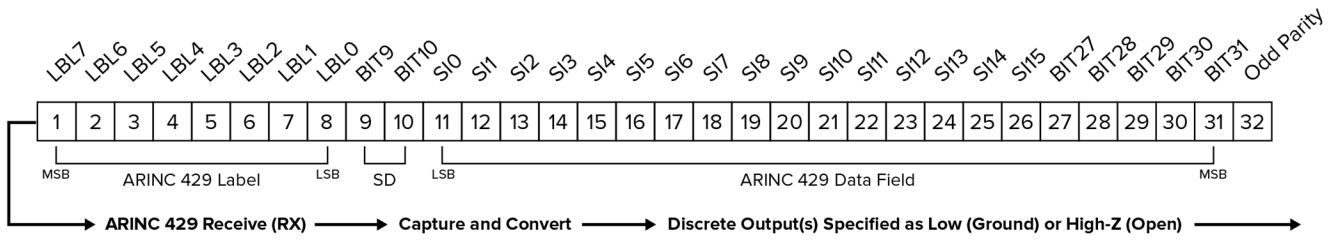
- ARINC 429 Signal Converters
- RS232/RS422 Transceiver Module

2.1.1 ARINC 429 Signal Converters

Summary Description

The NEXSYS ARINC 429 Signal Converter is either a Series N (8 Pin) or Series R (12 Pin) autonomous ARINC 429 receiver that includes the protocol logic necessary to capture and decode an ARINC 429 data word. The 32-bit data word is then converted into a discrete output, see Figure 2.1.1.0-A. Some configurations are also capable of performing interface solutions for encoding applications by performing the multi-bit decode operation.

Figure 2.1.1.0-A



The NEXSYS Signal Converter is available in three configuration types based on the requirements for data conversion and output control:

- Single-Bit Converter (SR429/1M), see Section 2.1.1.1
- Multi-Bit Converter (SR429/4M), see Section 2.1.1.2
- Multi-Bit Decoding Converter (SR429/4D), see Section 2.1.1.3

The simple input-pin interface does not rely on any microcontroller, software or firmware control, eliminating the qualification requirements of DO-178 or complex hardware (DO-254).

The NEXSYS ARINC 429 Signal Converter (SR429/1M, /4M, /4D) is a commercial-off-the-shelf (COTS) item. This standard catalog hardware includes features to allow for flexible interface design solutions while also meeting aircraft performance standards. The SR429 is designed, tested, and qualified to MIL-PRF-22885/116, MIL-PRF-22885/117, DO-160 and MIL-STD-461 requirements. Specifications are available in our MIL-PRF and DO-160 Documents page, and the qualification table is available in Appendix A.

Standard Input Characteristics

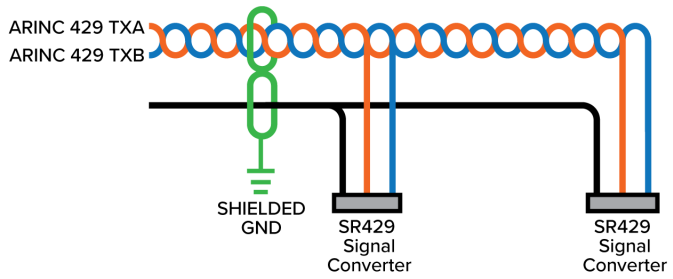
The NEXSYS ARINC 429 Signal Converter inputs are Power (28V), Ground (GND), Receive A (RXA) and Receive B (RXB). See additional sections for specific details concerning the Input/Output (I/O) interface. The inputs include the following characteristics for custom data conversion and output control. Input circuity is diode isolated, buffered, and debounced for reliable operation.

28V (PIN 4): Operating voltage (Nom.), 8 mA Current Draw (Max).
GND (PIN 5): Continuous Ground required, otherwise, inadvertent operation could occur.
RXA (PIN 2), RXB (PIN 3): Two-wire data Receive (RX) interface that autonomously receives the ARINC 429 unit of Transmission (TX).

RXA, RXB Installation Notes: The industry standard connection should include two wires that are twisted pairs with shielded ground cabling, which provides a balanced differential signal transmission. Multiple converters wire together, in parallel chain termination method, see Figure 2.1.1.0-B.

Note: ARINC 429 converters are tested to operate without twisted or shielding wires.

Figure 2.1.1.0-B



Standard ARINC 429 Configuration Options

The NEXSYS ARINC 429 Signal Converters can be customized to provide an application-specific control interface to other avionics equipment. Standard ARINC 429 data bus protocol and 32-bit word format options are configured, by utilizing the online Part Configurator.

Label: The specification of an octal (base-8) label (000-377). When energized, if a loss of data should occur, the converter latches the last valid transmission until valid data is once again received.

Data Bit(s): The specification of data bit (11-31) to be used as Discrete Outputs or to be used in Binary Outputs, see *Standard Output Characteristics*.

Source/Destination Identifiers (SDI): The specification to enable or disable (ignore) bits 9 and 10, used as an extension of the label for valid label identification.

Transmission Speed: The specification of the speed by which a converter receives (RX) the ARINC 429 unit of transmission (TX). The options are either High speed (100 kbps) or Low speed (12.5 kbps).

Standard Output Characteristics

NEXSYS Signal Converters (SR429/1M, SR429/4M, and SR429/4D) receive (RX) an ARINC 429 data transmission (TX), which is decoded and converted into active discrete output(s). One or more single (unary) bits in the ARINC 429 data word can be converted into discrete outputs, depending upon the configuration type that is specified. The available configuration types provide up to three distinct output control activation options; Discrete Outputs, Decoded Outputs and the Failure Output.

All outputs are open-drain High-Z (Open) when not active. The output load capacity is 1.0 A for the SR429/1M and 0.5 A for SR429/4M and SR429/4D , see Figure 2.1.1.4-A (Operating Parameters) for electrical load rating types.

Discrete Outputs: Two Active Output options are available when converting the unary ARINC data bit to a Discrete Output: Standard, High-Z (Open) when Bit = 1 or Inverted, or Low (Ground) when Bit = 1. When Bit = 0 the output is orthogonal to the specified level when Bit = 1, see Figure 2.1.1.0-C.

Figure 2.1.1.0-C

Output Option	DATA BIT (Value)	DISCRETE OUTPUT (Signal Level)
Standard	1	High-Z (Open)
	0	Low (Ground)
Inverted	1	Low (Ground)
	0	High-Z (Open)

Decoded Outputs - Active Outputs can also represent the Binary Decode (BD) of multiple bits, and the Decoded Outputs options are: the BD variations of two or three data bits in the SR429/4D or of the Sign/Status Matrix bits (30, 31) available in the SR429/4M. Active Decoded Outputs are specified as Low (Ground) or High-Z (Open) when the decode = *TRUE*, see Figure 2.1.1.0-D.

Figure 2.1.1.0-D

Output Option	BINARY DECODE (Variation)	DECODED OUTPUT (Signal Level)
Low (Ground) when Decode Variation = *TRUE*	BD = *TRUE*	Low (Ground)
	BD = *FALSE*	High-Z (Open)
High-Z (Open) when Decode Variation = *TRUE*	BD = *TRUE*	High-Z (Open)
	BD = *FALSE*	Low (Ground)

Data bits that are specified for the BD function are positioned from MSB (Most Significant Bit) to LSB (Least Significant Bit). The MSB may also function as the sign bit in the two's complement operation to represent a negative value (i.e., negative altitude, voltage, or temperature), with the addition of other NEXSYS components.

Failure Output - The NEXSYS ARINC 429 Signal Converter is also designed to monitor power and health of the internal IC receiver and offers two options for failure detection, Health and Watchdog, see Figure 2.1.1.0-E. Both options monitor the internal IC and produce an Active Output upon failure of the receiver IC and/or failure to receive valid ARINC data within a specified time buffer. The Health option also monitors loss of unit power.

Figure 2.1.1.0-E

Output Option	IC (Status)	FAILURE OUTPUT (Signal Level)
Health	NORM	Low (Ground)
	FAIL	High-Z (Open)
Watchdog	NORM	High-Z (Open)
	FAIL	Low (Ground)

Health and Watchdog include a buffer-timer that is intended to monitor that valid data is received within a specified time. Health and Watchdog timing is specified during part number configuration, and the options are 0.5 s, 1.0 s. 1.75 s, 2.5 s, 5.0 s, 10.0 s, 15.0 s.

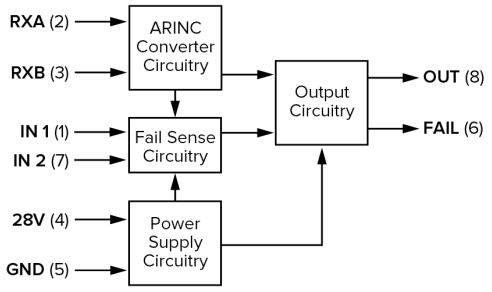
In the SR429/1M , only the Health version of the Failure Output is available which can be combined with additional external failure discretes to activate the Failure Output (FAIL, PIN 6), see "ARINC 429 Single-Bit Converter (SR429/1M)" on the facing page.

2.1.1.1 ARINC 429 Single-Bit Converter (SR429/1M)

The ARINC 429 Single-Bit Converter (SR429/1M) is a Series N (8 Pin) device that offers one Discrete Output (OUT, PIN 8) from a single bit and one Failure Output (FAIL, PIN 6) that activates when the Fail Sense Circuitry detects a failure condition, see Figure 2.1.1.1-A. Output options are shown below in table Figure 2.1.1.1-B.

The FAIL output (FAIL, PIN 6) from the Fail Sense Circuitry is a Health Failure Output, defined as Normal = Low (Ground) and Fail = High-Z (Open). The primary purpose of the FAIL output is to monitor the power and health of the internal IC. The Fail Sense Circuitry can be bypassed if unused.

Figure 2.1.1.1-A



SERIES N

See Figure 6.0.0.0-C for pinout variations by form factor

Optionally, the SR429/1M provides two (IN 1, PIN 1 and IN 2, PIN 7) independent failure inputs to the Fail Sense Circuitry that allows simultaneous monitoring of the internal IC health and signal level transitions from two external failure inputs. IN 1 and IN 2 are inputs with specific failure signal definitions.

- **IN 1 (PIN 1):** Triggers the FAIL output (PIN 6) upon a fixed input level transition from Normal = High, High-Z (Open) or > +20 VDC to Fail = Low (Ground) or < +6 VDC (↘). IN 1 may remain disconnected if unused.
- **IN 2 (PIN 7):** Triggers the FAIL output (PIN 6) upon one of two selectable input level transitions as described below (↘). IN 2 must remain connected to the specified Normal signal level if unused.
  - Normal = Low (Ground) or < +6 VDC to Fail = High, High-Z (Open) or > +20 VDC.
  - Normal = High, High-Z (Open) or > +20 VDC to Fail = Low (Ground) or < +6 VDC (similar to IN 1).

When either IN 1 or IN 2 detects a signal level transition as defined above, or the internal IC has failed, the FAIL output transitions from Normal = Low (Ground) to Fail = High-Z (Open).

Figure 2.1.1.1-B I/O OPTIONS

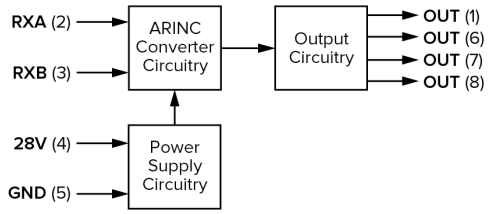
	Pin 6 (FAIL)	Pin 8 (OUT)
SERIES N	H	11 to 31
	OPTION DEFINITION	
	H	Failure Output (Health) is Fail = High-Z (Open).
	11 to 31	For a single-bit, 11 to 31 inclusive, Discrete Output can be specified as Standard = High-Z (Open) when Bit = 1 or Inverted = Low (Ground) when Bit = 1.

2.1.1.2 ARINC 429 Multi-Bit Converter (SR429/4M)

The ARINC 429 Multi-Bit Converter (SR429/4M) is available as a NEXSYS Series N (8 Pin) or Series R (12 Pin) signal converter.

- **Series N (8 Pin) SR429/4M:** Provides four Discrete or Failure Outputs (PINS 1, 6-8), see Figure 2.1.1.2-A. Discrete Outputs and Failure Outputs can be repeated to avoid external splicing. Output options for the four outputs are shown in detail, see Figure 2.1.1.2-C.

Figure 2.1.1.2-A

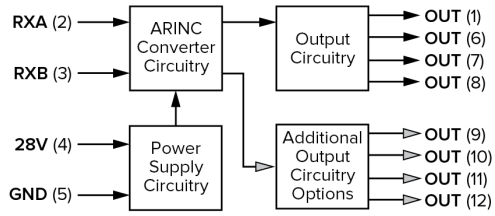


See Figure 6.0.0.0-C for pinout variations by form factor

SERIES N

- **Series R (12 Pin) SR429/4M:** Provides four Discrete or Failure Outputs (PINS 1, 6-8) plus four additional outputs (PINS 9-12), see Figure 2.1.1.2-B. Discrete Outputs and Failure Outputs can be repeated to avoid external splicing. The additional outputs (PINS 9-12) can be used as Decoded Outputs of the Sign/Status Matrix (SSM) bits 30 and 31 or as additional Discrete or Failure Outputs. When additional Discrete Outputs are specified, the signal levels will be the inverted value of the initial four Discrete Outputs. Output options, including the ability to repurpose SSM decode variation 00 (PIN 9) with additional data, are shown in detail in, see Figure 2.1.1.2-C.

Figure 2.1.1.2-B



See Figure 6.0.0.0-D for pinout variations by form factor

SERIES R

Figure 2.1.1.2-C I/O OPTIONS

	PIN 1	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	PIN 11	PIN 12
SERIES N	11 to 31, H or W	11 to 31, H or W	11-31, H or W	11 to 31, H or W	-	-	-	-
SERIES R	11 to 31, H or W	11 to 31, H or W	11 to 31, H or W	11 to 31	[9]	[10] or H	[11] or H	[12] or H
	11 to 31, H or W	11 to 31, H or W	11 to 31, H or W	H or W	H or W	[10] or H	[11] or H	[12] or H
	11 to 31, H or W	11 to 31, H or W	11 to 31, H or W	11 to 29	H or W	[10] or H	[11] or H	[12] or H
	11 to 29	11 to 29	11 to 29	11 to 31, H or W	SSM00	SSM01	SSM10	SSM11
	11 to 29	11 to 29	11 to 29	11 to 31, H or W	H or W	SSM01	SSM10	SSM11
	11 to 29	11 to 29	11 to 29	11 to 31	[9]	SSM01	SSM10	SSM11
	11 to 29	11 to 29	11 to 29	H or W	H or W	SSM01	SSM10	SSM11

OPTION DEFINITION	
11 to 29, 11 to 31	For a single bit, 11 to 29 or 11 to 31 inclusive, Discrete Output can be specified as Standard = High-Z (Open) when Bit = 1 or Inverted = Low (Ground) when Bit = 1.
H	Failure Output is High-Z (Open) when Health Monitor = Fail.
W	Failure Output is Low (Ground) when Watchdog = Fail.
[9]	Will be the same Bit specified on PIN 8, Discrete Output can be specified as Standard = High-Z (Open) when Bit = 1 or Inverted = Low (Ground) when Bit = 1 regardless of output selection for PIN 8.
[10]	Will be the same Bit specified on PIN 7, Discrete Output is Inverted = Low (Ground) regardless of output selection for PIN 7.
[11]	Will be the same Bit specified on PIN 6, Discrete Output is Inverted = Low (Ground) regardless of output selection for PIN 6.
[12]	Will be the same Bit specified on PIN 1, Discrete Output is Inverted = Low (Ground) regardless of output selection for PIN 1.
SSM00 to SSM11	Binary Decode of SSM Bits (Bits 30 and 31), Binary Outputs can be specified as High-Z (Open) when DECODE = *TRUE* or Inverted = Low (Ground) when DECODE = *TRUE*.

Note: [ ] Bracket denotes Pin Number.

2.1.1.3 ARINC 429 Multi-Bit Decoding Converter (SR429/4D)

The ARINC 429 Multi-Bit Decoding Converter (SR429/4D) is available as a NEXSYS Series N (8 Pin) or Series R (12 Pin) component.

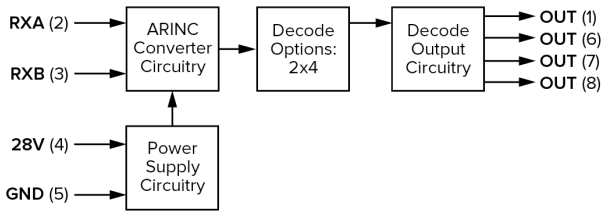
The SR429/4D can be configured in two standard types of decoding:

- **2 x 4 Decoder:** Performs a Binary Decode (BD) of two ARINC data bits producing four Decoded Outputs. The 2 X 4 Decoding Converter can be configured as a Series N (8 Pin) device, see Figure 2.1.1.3-A or a Series R (12 Pin) device with additional outputs, see Figure 2.1.1.3-B.
- **3 x 8 Decoder:** Performs a Binary Decode (BD) of three ARINC data bits producing eight Decoded Outputs. The 3 X 8 Decoding Converter is configured as a Series R (12 Pin) device, see Figure 2.1.1.3-D. BD variations 000 and/or 111 can be repurposed as Discrete or Failure Outputs.

SR429/4D with 2 x 4 Decoder

- **Series N (8 Pin) 2 x 4 Decoder:** Four Decoded Outputs (PINS 1, 6-8); each output is a Binary Decode (BD) variation (00, 01, 10, 11) of two bits according to the ARINC 429 word protocol, see Figure 2.1.1.3-A. Output options include the ability to repurpose the BD variation 00 (PIN 1) and/or the BD variation 11 (PIN 8) with additional data, see Figure 2.1.1.3-C.

Figure 2.1.1.3-A

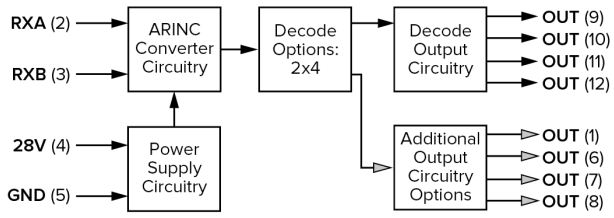


See Figure 6.0.0.0-C for pinout variations by form factor

SERIES N

- **Series R (12 Pin) 2 x 4 Decoder:** Eight total outputs. Four Decoded Outputs (PINS 9-12); each output is a Binary Decode (BD) variation (00, 01, 10, 11) of two bits according to the ARINC 429 word protocol, see Figure 2.1.1.3-B. Additional output options include the ability to repurpose the BD variation 00 (PIN 9) and/or the BD variation 11 (PIN 12) with additional data. Four additional outputs (PIN 1, 6-8) are available for Discrete or Failure Outputs, see Figure 2.1.1.3-C for detail of the output options for all Series R pins.

Figure 2.1.1.3-B



See Figure 6.0.0.0-D for pinout variations by form factor

SERIES R

Figure 2.1.1.3-C I/O OPTIONS

	PIN 1	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	PIN 11	PIN 12
SERIES N	DEC00	DEC01	DEC10	DEC11	-	-	-	-
	11 to 29	DEC01	DEC10	DEC11	-	-	-	-
	DEC00	DEC01	DEC10	11 to 31, H or W	-	-	-	-
	11 to 29	DEC01	DEC10	11 to 31, H or W	-	-	-	-
SERIES R	11 to 29	MSB (11 to 31, H, W)	LSB (11 to 31, H, W)	11 to 31, H or W	DEC00	DEC01	DEC10	DEC11
	11 to 29	MSB (11 to 31, H, W)	LSB (11 to 31, H, W)	11 to 31	[9]	DEC01	DEC10	DEC11
	11 to 29	MSB (11 to 31, H, W)	LSB (11 to 31, H, W)	H or W	H or W	DEC01	DEC10	DEC11
	11 to 29	MSB (11 to 31, H, W)	LSB (11 to 31, H, W)	11 to 29	H or W	DEC01	DEC10	DEC11

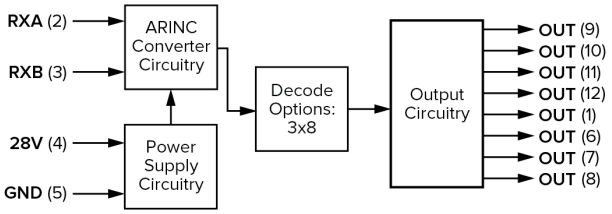
OPTION DEFINITION	
DEC00 to DEC11	Binary decode variations for specified label and bits; Binary Outputs can be specified as Low (Ground) or High-Z (Open) when DECODE = *TRUE*.
11 to 29, 11 to 31	For a single bit, 11 to 29 or 11 to 31 inclusive, Discrete Output can be specified as Standard = High-Z (Open) when Bit = 1 or Inverted = Low (Ground) when Bit = 1.
H	Failure Output is High-Z (Open) when Health Monitor = Fail.
W	Failure Output is Low (Ground) when Watchdog = Fail.
[9]	Must be the same Bit specified on PIN 8, Discrete Output can be specified as Standard = High-Z (Open) when Bit = 1 or Inverted = Low (Ground) when Bit = 1 regardless of output selection for PIN 8.
MSB, LSB	Discrete Output of Most/Least significant bit used in 2 x 4 decoder. Discrete Outputs can be specified as Standard = High-Z (Open) when Bit = 1 or Inverted = Low (Ground) when Bit = 1.

Note: [ ] Bracket denotes Pin Number.

SR429/4D with 3X8 Decoder

- **Series R (12 Pin) 3 x 8 Decoder:** Eight Binary Outputs (PINS 1, 6-12); each output is a Binary Decode (BD) variation (000, 001, 010, 011, 100, 101, 110, 111) of three bits according to the ARINC 429 word protocol, see Figure 2.1.1.3-D. Output options include the ability to repurpose the BD variation 000 (PIN 9) and/or the BD variation 111 (PIN 8) with additional data, see Figure 2.1.1.3-E.

Figure 2.1.1.3-D



See Figure 6.0.0.0-D for pinout variations by form factor

SERIES R

Figure 2.1.1.3-E I/O OPTIONS

	PIN 9	PIN 10	PIN 11	PIN 12	PIN 1	PIN 6	PIN 7	PIN 8
SERIES R	DEC000	DEC001	DEC010	DEC011	DEC100	DEC101	DEC110	DEC111
	11 to 31, H or W	DEC001	DEC010	DEC011	DEC100	DEC101	DEC110	DEC111
	DEC000	DEC001	DEC010	DEC011	DEC100	DEC101	DEC110	11 to 31, H or W
	[9]	DEC001	DEC010	DEC011	DEC100	DEC101	DEC110	11 to 31
	H or W	DEC001	DEC010	DEC011	DEC100	DEC101	DEC110	11 to 29, H or W
	DEC000	DEC001	DEC010	DEC011	DEC100	DEC101	DEC110	DEC111
	11 to 31, H or W	DEC001	DEC010	DEC011	DEC100	DEC101	DEC110	DEC111
	DEC000	DEC001	DEC010	DEC011	DEC100	DEC101	DEC110	11 to 31, H or W

OPTION DEFINITION	
DEC000 to DEC111	Binary decode variations for specified label and bits; Binary Outputs can be specified as Low (Ground) or High-Z (Open) when DECODE = *TRUE*.
11 to 29, 11 to 31	For a single bit, 11 to 29 or 11 to 31 inclusive, Discrete Output can be specified as Standard = High-Z (Open) when Bit = 1 or Inverted = Low (Ground) when Bit = 1.
H	Failure Output is High-Z (Open) when Health Monitor = Fail.
W	Failure Output is Low (Ground) when Watchdog = Fail.
[9]	Must be the same Bit specified on PIN 8, Discrete Output can be specified as Standard = High-Z (Open) when Bit = 1 or Inverted = Low (Ground) when Bit = 1 regardless of output selection for PIN 8.

Note: [ ] Bracket denotes Pin Number.

2.1.1.4 ARINC 429 Signal Converters, Operating Parameters

Figure 2.1.1.4-A	
Description	Parameters
Operating Parameters	
Operating Voltage (Max./Nom./ Min.)	+32 VDC /+28 VDC/+18 VDC
Power Supply Input Current	8 mA (Maximum)
Reset Time from Power Loss at 25°C	5 sec (Minimum)
Hold Up Time from Power Loss at 25°C	200 ms (Minimum)
Input Parameters	
IN 1, IN 2 **(SR429/1M)** Input Timing at 25°C	5 ms (Typical)
IN 1, IN2 **(SR429/1M)** Low Level Input Current (I_{IL}) at 25°C	1 mA (Maximum)
* IN 1, IN 2 **(SR429/1M)** Low Level Input Voltage (V_{IL}) at 25°C	< +6 VDC
* High **(SR429/1M)** Level Input Voltage (V_{IH}) at 25°C	> +20 VDC
ARINC 429 Inputs **(SR429/1M, SR429/4M, SR429/4D)**	IAW ARINC 429 Protocol
IN 1, IN 2 inputs are diode isolated	
Output Parameters	
Output Load Capacity	**SR429/1M:** Fused MOSFET - 1.0 A (Resistive), 0.5 A (Motor/Inductive/Lamp) **SR429/4M, SR429/4D:** IntelliFET® 0.5 A (Resistive/Motor/Inductive/Lamp)
On-State Resistance at 25°C	**SR429/1M:** Typical 0.07 ohms / Maximum 0.09 ohms **SR429/4M, SR429/4D:** Typical 0.4 ohms / Maximum 0.6 ohms
Off-State Resistance at 25°C	**SR429/1M:** Open Drain (High-Z), Fuse-Protected MOSFET, +32 VDC Maximum **SR429/4M, SR429/4D:** Open Drain (High-Z), Self-Protected IntelliFET®, +32 VDC Maximum
Temperature	
Operating Temperature	-55°C to +85°C
Non-Operating Temperature	-55°C to +125°C
Reliability MIL-HDBK-217F, Notice 2	
Airborne Inhabited Cargo (AIC) at +40°C Continuous Operation	**SR429/1M** MTBF = 116,317 hrs **SR429/4M, SR429/4D** MTBF = 103,012 hrs
** V_{IL} and V_{IH} specifications are in reference to unit Ground.*	

For Qualification Summary, see Appendix A.

2.1.2 RS232/RS422 Transceiver Module

Summary Description

The NEXSYS RS232/RS422 Transceiver Module is a standalone, bidirectional device designed to interface with the NEXSYS LYNK Integrated Signal Processor (ISP) for seamless data exchange, robust signal integrity, and exceptional reliability in demanding aviation environments. The module can transmit and receive signals between RS232 and RS422 data buses, supporting protocol communication at data rates from 2,400 bps to 115.2 kbps.

Engineered to meet rigorous avionics standards, this high-reliability transceiver preserves signal integrity and ensures consistent performance under extreme conditions, complying with MIL-PRF-22885/116 and RTCA/DO-160G specifications. With a propagation delay of less than 1.6 µs, it delivers reliable, industry-leading signal performance and precise speed matching, making it ideal for integration into time-sensitive aviation systems.

Standard Characteristics

Designed for reliable operation in demanding aerospace environments with the following interface options.

28V: Operating voltage (nom.), 8 mA current draw (max.)

GND: Dedicated ground connection required for stable operation

RS232 RX: Receive connection

RS232 TX: Transmit connection

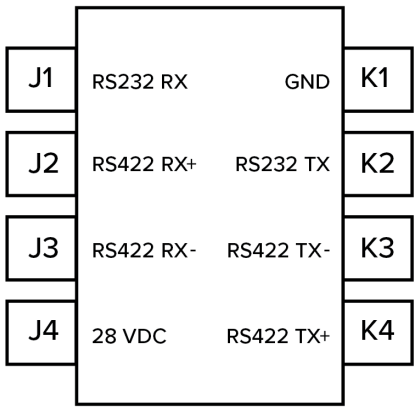
RS422 RX(+): Receive, positive connection (differential)

RS422 RX(-): Receive, negative connection (differential)

RS422 TX(+): Transmit, positive connection (differential)

RS422 TX(-): Transmit, negative connection (differential)

Figure 2.1.2.0-A



Configuration Options

Engineered to interface with NEXSYS product lines, the module uses a 22-pin CTS connector and supports direct integration with NEXSYS Component Technology devices and especially NEXSYS LYNK Integrated Signal Processors (ISP).

RS232 Characteristics: Industry-standard (EIA/TIA-232-E) RS232 interface specifications.

Figure 2.1.2.0-B

Characteristic	Conditions	Minimum	Nominal	Maximum
Input Resistance	Operation	3kΩ	5kΩ	7kΩ
Input Resistance	Input power = 0V	6kΩ	11kΩ	16kΩ
Input Hysteresis	-	-	0.5V	-
Output Voltage Swing	-	-	±5V	±5.5V
Output Short-Circuit Current	RS232 TX = Ground	-	±30 mA	±60 mA
Data Rate	RL = 3kΩ, CL = 1000pF	2400 bps	-	115.2 kbps
Cable Length	-	-	-	30m/100ft

RS422 Characteristics: Industry-standard RS422 interface specifications.

Figure 2.1.2.0-C

Characteristic	Conditions	Minimum	Nominal	Maximum
Input Resistance	-7V < VCM < +12V	96kΩ	-	-
Input Hysteresis	-	-	30 mV	-
Output Voltage Swing	-	±5V	±5.5V	-
Output Short-Circuit Current	RS232 TX = Ground		±30 mA	±60 mA
RTS	Voltage Input High (VIH)	2.4V	-	-
	Voltage Input Low (VIL)	-	-	0.8V
Differential Output Voltage (VOD)	R=50Ω (RS-422)	2	-	-
Data Rate	RL = 3kΩ, CL = 1000pF	2400 bps	-	115.2 kbps
Cable Length	-	-	-	30m/100ft

2.1.2.1 RS232/RS422 Transceiver Module, Operating Parameters

Figure 2.1.2.1-A	
Description	Parameters
Operating Parameters	
Operating Voltage (Max./Nom./ Min.)	+32 VDC /+28 VDC/+18 VDC
Power Supply Input Current	50 mA (Maximum)
Hold Up Time from Power Loss at 25°C	200 ms (Minimum)
Temperature	
Operating Temperature	-55°C to +85°C
Non-Operating Temperature	-55°C to +125°C
Reliability MIL-HDBK-217F, Notice 2	
Airborne Inhabited Cargo (AIC) at +40°C Continuous Operation	100,000 hrs (Minimum)

For Qualification Summary, see Appendix A.

2.2 Signal Switching/Control Components

Components that perform either direct or logically controlled switching using digital electronic circuitry such as Boolean logic gate operations.

Signal Switching/Control components include:

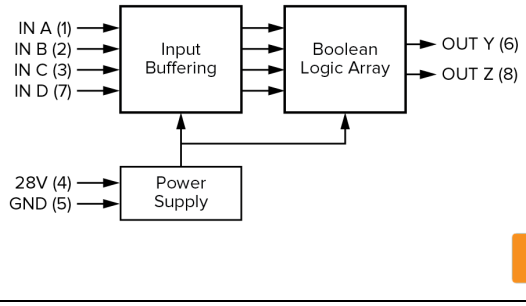
- Defined Logic
- Solid State Relay

2.2.1 Defined Logic

Summary Description

NEXSYS Defined Logic components consist of four configuration types of a Series C (8 Pin) component. The two input/four output interface (Figure 2.2.1.0-A) is designed to function as a digital electronic circuit controller that can perform Boolean logic gate operations *AND, OR, NOT, NAND, NOR, XOR, XNOR*, as well as *BUFFER*. The robust internal circuitry performs exceptionally well for use in wave and pulse shaping applications, as is typical in high-noise environments. Additional Defined Logic applications include Binary (BNR) and Binary-Coded Decimal (BCD) encoding for use in computing and other digital electronic circuit applications.

Figure 2.2.1.0-A



The NEXSYS Defined Logic (DL1, DL2, DL3, DL4) is a commercial-off-the-shelf (COTS) item. This standard catalog hardware includes features to allow for flexible interface design solutions while also meeting aircraft performance standards. The DL is designed, tested, and qualified to MIL-PRF-22885/116, MIL-PRF-22885/117, DO-160 and MIL-STD-461 requirements. Specifications are available in our MIL-PRF and DO-160 Documents page, and the qualification table is available in Appendix A.

There are four configuration types:

- Defined Logic 1 (DL1) is a combinational logic gate device that performs an Exclusive-OR (XOR) and Exclusive-NOR (XNOR) by decoding two (tied) pairs of four logic inputs to control two orthogonal outputs.
- Defined Logic 2 (DL2) decodes two independent Boolean logic gates (Channel 1 and 2). Each gate has two inputs that control one dedicated output.
- Defined Logic 3 (DL3) is a combinational Boolean logic gate device that decodes two independent logic gates, which cascade to a third gate to control two orthogonal outputs.
- Defined Logic 4 (DL4) is a combinational Boolean logic gate device that decodes four inputs to control two orthogonal outputs.

Input Characteristics

NEXSYS Defined Logic inputs are Power (28V), Ground (GND) and Logic Inputs (A, B, C, D). Defined Logic input circuity is diode isolated, buffered, and debounced for reliable operation. See additional sections for specific details concerning the Input/Output (I/O) interface. The inputs include the following characteristics for custom Boolean logic circuit control.

28V (PIN 4): Operating Voltage (Nom.), 4 mA Current Draw (Max.).
GND (PIN 5): Continuous Ground required, otherwise, inadvertent operation could occur.
A (PIN 1), B (PIN 2), C (PIN 3), D (PIN 7): Digital electronic inputs that detect logic level signals (1 or 0).

Input Options and Characteristics

NEXSYS Defined Logic inputs will detect signal levels that are present upon power-up. The input options involve specifying Pins A and C as either Pull-up or Pull-down to define the detected logic levels. Default levels are detected as either Logic High (1) or Logic Low (0) when the input signal is not active. For the DL1 variant only, inputs A and C are specified identically (Pull-up or Pull-down) since they are wired together externally. Inputs B and D are factory-configured and fixed as Pull-up.

The following describes the logic level detection options of inputs A and C and the fixed logic level detection definitions of inputs B and D. Configuring a Defined Logic part number to meet specific application requirements is accomplished by utilizing the online Part Configurator.

Inputs A and C, specified as Pull-up (U): The logic level is detected as Logic High (1) when above +4 VDC or High-Z (Open), and a Logic Low (0) when below +1.2 VDC.

Inputs A and C, specified as Pull-down (D): The logic level is detected as Logic High (1) when above +4 VDC, and a Logic Low (0) when below +1.2 VDC or High-Z (Open).

Inputs B and D, fixed as Pull-up (U): The signal level is detected as Logic High (1) when it is above +4 VDC or High-Z (Open), and a Logic Low (0) when below +1.2 VDC.

Note: If the input signal level transitions between +28 VDC and Low (Ground), either Pull-up or Pull-down may be specified since the High-Z (Open) level does not occur. If an input remains unused, the detected signal level (0 or 1) is defined by its Pull-up or Pull-down configuration.

Output Characteristics

NEXSYS Defined Logic active output signal levels are designated as 1 or 0, similar to input logic levels. However, output level definitions differ from the inputs, which are also designated as either 1 or 0. The following defines the Active Output signal levels.

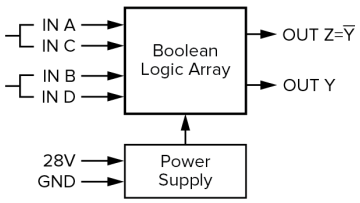
Active High-Z (Open), (1) Output: The output signal level is defined as High-Z (Open).
Active Low (Ground), (0) Output: The output signal level is defined as Ground.

Note: All outputs are open-drain High-Z (Open) when not active and, therefore, do not require external sneak path isolation circuitry. The output load capacity is 2.0 A, see Figure 2.2.1.5-A (Operating Parameters) for electrical load rating types.

2.2.1.1 Defined Logic 1 (DL1)

The Defined Logic 1 (DL1) is a combinational logic gate device that decodes two (tied) pairs of four logic inputs to control two orthogonal outputs, see Figure 2.2.1.1-A.

Figure 2.2.1.1-A



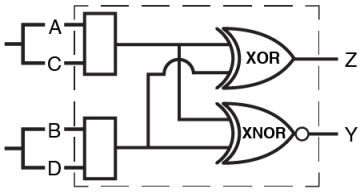
Application Performance

The DL1 is a digital electronic logic circuit controller that performs the Exclusive-*OR (XOR)* and Exclusive-*NOR (XNOR)* logic gate operations. OUT Y is Active High (1) or High-Z (Open) when both pairs of inputs are identical, and Active Low (0) or Ground when one pair is Low (0), and the other pair is High (1), Z is the complement of Y.

Combinational Logic Gate Options

The DL1 combines logic gates to implement digital circuits that solve more complex functions. For example, the gate-level digital circuit diagram below demonstrates how the *XOR* and *XNOR* operations are performed, see Figure 2.2.1.1-B. The *XOR* and *XNOR* logic gate operations are dedicated functions integral to the DL1, and both are performed in a single component.

Figure 2.2.1.1-B



With Inputs, AC externally wired together and BD externally wired, OUT Z performs the *XOR=TRUE* expression *if* AC *OR* BD is High (1), but not both. Conversely, with Inputs, AC externally wired together and BD externally wired, OUT Y performs the *XNOR=TRUE* expression if AC *OR* BD is High (1), but not both. Figure 2.2.1.1-C, Figure 2.2.1.1-D, and Figure 2.2.1.1-E define the *XOR* and *XNOR=TRUE* expressions and logic statements.

Figure 2.2.1.1-C

XOR Gate Symbol		Expression: *XOR=TRUE*	
		The Exclusive-*OR* (*XOR*) gate produces an Active Open (1) output if either, but not both, of its inputs is High (1).	
Equation	Variation	TRUTH TABLE	Boolean Logic "if" Statement
Z = AC ⊕ BD		**A,C:** 0 0 1 1 **B,D:** 0 1 0 1 **Y :** 1 0 0 1 **Z :** 0 1 1 0	if AC is High (1) *OR* BD is High (1), then Z is Open (1) else Z is Ground (0), Y is the complement of Z.

Figure 2.2.1.1-D

XNOR Gate Symbol		Expression: *XNOR=TRUE*	
		The Exclusive-*NOR* (*XNOR*) gate produces an Active Ground (0) output if either, but not both, of its inputs is High (1).	
Equation	Variation	TRUTH TABLE	Boolean Logic "if" Statement
Y = $\overline{AC \oplus BD}$		**A,C:** 0 0 1 1 **B,D:** 0 1 0 1 **Y :** 1 0 0 1 **Z :** 0 1 1 0	if AC is High (1) *OR* BD is High (1), Y is Ground (0) else Y is Open (1), Z is the complement of Y.

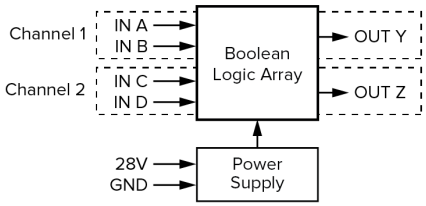
Figure 2.2.1.1-E

Inputs		Outputs: 1 = High-Z (Open), 0 = Low (Ground)	
		XOR	XNOR
A , C	B , D	$Z = AC \oplus BD$	$Y = \overline{AC \oplus BD}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

2.2.1.2 Defined Logic 2 (DL2)

The Defined Logic 2 (DL2) decodes two independent Boolean logic gates (Channel 1 and 2). Each gate has two inputs that control one dedicated output, see Figure 2.2.1.2-A

Figure 2.2.1.2-A



Application Performance

The DL2 is a digital electronic logic circuit controller that performs up to ten Boolean logic gate operations. The device allows the design flexibility of an independent, dual-channel device while also affording the wiring efficiencies of common power for both channels. Channel 1 consists of inputs A and B, which control OUT Y. Channel 2 consists of inputs C and D, which control OUT Z. Logic gate decodes are defined in the following truth table, see Figure 2.2.1.2-B - Figure 2.2.1.2-G, and Figure 2.2.1.2-H.

Boolean Logic Gate Options

The DL2 interface can function as a two-channel digital electronic circuit controller to perform the Boolean logic gate operations *AND, OR, NOT, NAND, NOR, XOR, XNOR*, as well as *BUFFER*. Each device consists of four inputs (A, B, C, D) and two outputs (Y,Z). The following tables detail the two-input logic gate operation of the DL2. Each channel has four variations, except *BUFFER*, and *NOT*. While digital notations also exist for equation Z = CD (Channel 2) , only Y = AB and Y = A (Channel 1) are depicted for simplicity, see Figure 2.2.1.2-B - Figure 2.2.1.2-G. The complete truth table for each Boolean logic gate operation is calculated as selections are made with the Part Configurator. The Boolean logic gate variations identified below are assigned based on part configuration. Variation number four, *AND* (4) and *NOR* (4), result in a logic gate equivalency (4=4). Likewise, variations specified as number eight, *NAND* (8) and OR (8), result in a logic gate equivalency (8=8). The following DL2 Boolean logic gate operations are also used to specify the first selection of the DL3 combinational logic circuit, see "Defined Logic 3 (DL3)" on page 27.

Figure 2.2.1.2-B

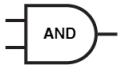
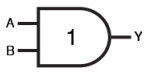
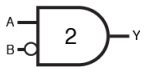
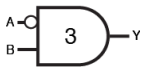
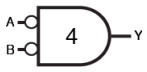
AND Gate Symbol		Boolean Expression: *AND=TRUE*	
		The *AND* gate produces an Active Open (1) output only if all inputs are High (1).	
Equation	Variation	TRUTH TABLE	Boolean Logic "if" Statement for Variations
Y = A • B		**A:** 0 0 1 1 **B:** 0 1 0 1 **Y:** 0 0 0 1	if A is High (1) *AND* B is High (1), then Y is Open (1) else Y is Ground (0).
Y = A • $\overline{B}$		**A:** 0 0 1 1 **B:** 0 1 0 1 **Y:** 0 0 1 0	if A is High (1) *AND* B is Low (0), then Y is Open (1) else Y is Ground (0).
Y = $\overline{A}$ • B		**A:** 0 0 1 1 **B:** 0 1 0 1 **Y:** 0 1 0 0	if A is Low (0) *AND* B is High (1), then Y is Open (1) else Y is Ground (0).
Y = $\overline{A}$ • $\overline{B}$		**A:** 0 0 1 1 **B:** 0 1 0 1 **Y:** 1 0 0 0	if A is Low (0) *AND* B is Low (0), then Y is Open (1) else Y is Ground (0).

Figure 2.2.1.2-C

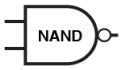
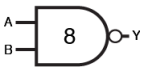
NAND Gate Symbol		Expression: *NAND=TRUE*	
		The *NOT-AND* (*NAND*) gate is equal to an *AND* gate followed by a *NOT* gate. The *NAND* gate produces an Active Open (1) output if any of the inputs are Low (0).	
Equation	Variation	TRUTH TABLE	Boolean Logic "if" Statement
$Y = \overline{A \cdot B}$		**A:** 0 0 1 1 **B:** 0 1 0 1 **Y:** 1 1 1 0	if A is High (1) *AND* B is High (1), then Y is Ground (0) else Y is Open (1).

Figure 2.2.1.2-D

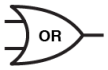
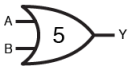
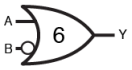
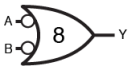
OR Gate Symbol		Boolean Expression: *OR=TRUE*	
		The *OR* gate produces an Active Open (1) output if ***one OR more*** of its inputs are High (1).	
Equation	Variation	TRUTH TABLE	Boolean Logic "if" Statement for Variations
Y = A + B		**A:** 0 0 1 1 **B:** 0 1 0 1 **Y:** 0 1 1 1	if A is High (1) *OR* B is High (1), then Y is Open (1) else Y is Ground (0).
Y = A + $\overline{B}$		**A:** 0 0 1 1 **B:** 0 1 0 1 **Y:** 1 0 1 1	if A is High (1) *OR* B is Low (0), then Y is Open (1) else Y is Ground (0).
$\overline{A}$ + B		**A:** 0 0 1 1 **B:** 0 1 0 1 **Y:** 1 1 0 1	if A is Low (0) *OR* B is High (1), then Y is Open (1) else Y is Ground (0).
$\overline{A}$ + $\overline{B}$		**A:** 0 0 1 1 **B:** 0 1 0 1 **Y:** 1 1 1 0	if A is Low (0) *OR* B is Low (0), then Y is Open (1) else Y is Ground (0).

Figure 2.2.1.2-E

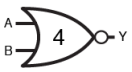
NOR Gate Symbol		Expression: *NOR=TRUE*	
		The *NOT-OR* (*NOR*) gate is equal to an *OR* gate followed by a *NOT* gate. The *NOR* gate produces an Active Ground (0) output if any of the inputs are High (1).	
Equation	Variation	TRUTH TABLE	Boolean Logic "if" Statement
$Y = \overline{A + B}$		**A:** 0 0 1 1 **B:** 0 1 0 1 **Y:** 1 0 0 0	if A is High (1) *OR* B is High (1), then Y is Ground (0) else Y is Open (1).

Figure 2.2.1.2-F

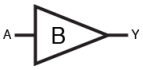
BUFFER Gate Symbol		Expression: *BUFFER=TRUE*	
		The *BUFFER* gate passes a filtered state of the input to its output.	
Equation	Variation	TRUTH TABLE	Boolean Logic "if" Statement
Y = A		**A:** 0 1 **Y:** 0 1	if A is High (1), then Y is Open (1); if A is Low (0), then Y is Ground (0).

Figure 2.2.1.2-G

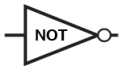
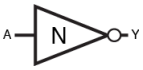
NOT Gate Symbol		Expression: *NOT=TRUE*	
		The *NOT* gate produces an inverted version of the input at its output. It is also known as an *INVERTER*. If the input variable is A, the inverted output is known as *NOT* A.	
Equation	Variation	TRUTH TABLE	Boolean Logic "if" Statement
Y = $\overline{A}$		**A:** 0 1 **Y:** 1 0	if A is High (1), then Y is Ground (0); if A is Low (0), then Y is Open (1).

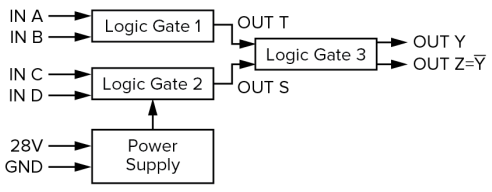
Figure 2.2.1.2-H

Inputs		Y Output (Channel 1): 1 = High-Z (Open), 0 = Low (Ground)									
		1	2	3	4	5	6	7	8	B	N
A	B	A•B	A•$\overline{B}$	$\overline{A}$•B	$\frac{\overline{A}\cdot\overline{B}}{A+B}$	A+B	A+$\overline{B}$	$\overline{A}$+B	$\frac{\overline{A}+\overline{B}}{A\cdot B}$	Buffer Y=A	Inverter Y=$\overline{A}$
0	0	0	0	0	**1**	**0**	1	1	**1**	0	1
0	1	0	0	**1**	0	1	**0**	1	**1**	0	1
1	0	0	**1**	0	0	1	1	**0**	**1**	1	0
1	1	**1**	0	0	0	1	1	1	**0**	1	0
Inputs		**Z Output (Channel 2): 1 = High-Z (Open), 0 = Low (Ground)**									
		1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**B**	**N**
C	**D**	C•D	C•$\overline{D}$	$\overline{C}$•D	$\frac{\overline{C}\cdot\overline{D}}{C+D}$	C+D	C+$\overline{D}$	$\overline{C}$+D	$\frac{\overline{C}+\overline{D}}{C\cdot D}$	Buffer Z=C	Inverter Z=$\overline{C}$
0	0	0	0	0	**1**	**0**	1	1	**1**	0	1
0	1	0	0	**1**	0	1	**0**	1	**1**	0	1
1	0	0	**1**	0	0	1	1	**0**	**1**	1	0
1	1	**1**	0	0	0	1	1	1	**0**	1	0

2.2.1.3 Defined Logic 3 (DL3)

The Defined Logic 3 (DL3) is a combinational logic gate device that decodes two independent logic gates, which cascade to a third gate to control two orthogonal outputs, see Figure 2.2.1.3-A.

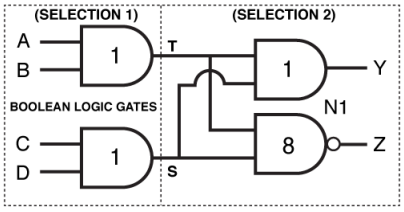
Figure 2.2.1.3-A



Application Performance

The DL3 is a digital electronic logic circuit controller that performs cascaded Boolean logic gate operations. The device reduces the necessity of multiple components and wiring complexity by cascading three logic gate operations internal to the device. Logic Gate 1 (T) and Logic Gate 2 (S) operate as independent logic gates that are decoded and then cascaded into a third logic gate, which is decoded to control the two outputs (YZ). OUT Y (Logic Gate 3) is normally Active Low (0) or Ground until the decode of Logic Gate 1 (T) and Gate 2 (S) is *TRUE*, as determined by the specified configuration, Z is the complement of Y.

Figure 2.2.1.3-B



Combinational Logic Gate Options

The DL3 combines logic gates to reduce the number of gates (components) required for implementation in a logic circuit. The DL3 builds upon the functionality of the DL2. First, two independent Boolean logic gates are specified (Selection 1, see Figure 2.2.1.3-B.) using the same options offered for the DL2, see Figure 2.2.1.2-B - Figure 2.2.1.2-G. The results of the two Boolean logic gates (TS) are then cascaded into a third combinational gate (N1-N4) to represent the sum-of-products, to perform multiple logic gate operations. For example, two *AND* gates (AB, CD) can be interfaced to a combination logic gate (N1) to produce the results of the outputs (YZ), see Figure 2.2.1.3-B.

The gate-level digital circuit diagrams below (N1-N4) represent the combinational logic gate operations available with the DL3, see Figure 2.2.1.3-C - Figure 2.2.1.3-F and Figure 2.2.1.3-G. Each option (N1-N4) combines and decodes any variation of two Boolean logic gate operations, as defined in the DL2 section (Figure 2.2.1.2-B - Figure 2.2.1.2-G). Complete logic tables representing all combinational gate operations are calculated as selections are made with the Part Configurator. Both N1 combinational logic gate variations result in logic gate equivalences (N1=N1), as well as both N4 variations (N4=N4). The combinational logic gate variation N1 is the logical inverse of N4 ($\overline{N1}$=N4), and N2 is the complement binary form (1's complement) of the N3 variation.

Figure 2.2.1.3-C

Expression: N1 = *TRUE*

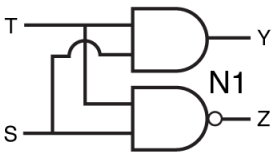
Equation	Variation	TRUTH TABLE	Boolean Logic "if" Statement for Variations
$Y = T \cdot S$ $Z = \overline{T \cdot S}$		**T:** 0 0 1 1 **S:** 0 1 0 1 **Y:** 0 0 0 1 **Z:** 1 1 1 0	if T is High (1) *AND* S is High (1), then Y is Open (1) else Y is Ground (0), Z is the complement of Y.

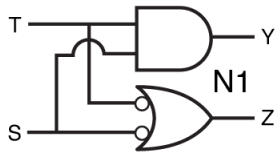
Figure 2.2.1.3-C (cont'd)			
Expression: N1 = *TRUE*			
Equation	Variation	TRUTH TABLE	Boolean Logic "if" Statement for Variations
$Y = T \bullet S$ $Z = \overline{T} + \overline{S}$		**T:** 0 0 1 1 **S:** 0 1 0 1 **Y:** 0 0 0 1 **Z:** 1 1 1 0	if T is High (1) *AND* S is High (1), then Y is Open (1) else Y is Ground (0), Z is the complement of Y.

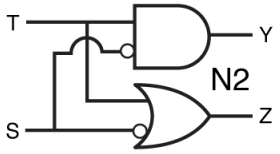
Figure 2.2.1.3-D			
Expression: N2=*TRUE*			
Equation	N2	TRUTH TABLE	Boolean Logic "if" Statement
$Y = T \bullet \overline{S}$ $Z = T + \overline{S}$		**T:** 0 0 1 1 **S:** 0 1 0 1 **Y:** 0 0 1 0 **Z:** 1 1 0 1	if T is High (1) *AND* S is Low (0), then Y is Open (1) else Y is Ground (0), Z is the complement of Y.

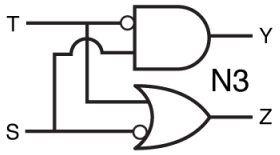
Figure 2.2.1.3-E			
Expression: N3=*TRUE*			
Equation	N3	TRUTH TABLE	Boolean Logic "if" Statement
$Y = \overline{T} \bullet S$ $Z = T + \overline{S}$		**T:** 0 0 1 1 **S:** 0 1 0 1 **Y:** 0 1 0 0 **Z:** 1 0 1 1	if T is Low (0) *AND* S is High (1), then Y is Open (1) else Y is Ground (0), Z is the complement of Y.

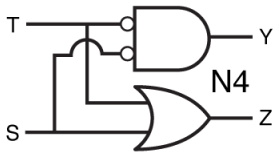
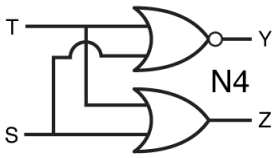
Figure 2.2.1.3-F			
Expression: N4=*TRUE*			
Equation	Variation	TRUTH TABLE	Boolean Logic "if" Statement for Variations
$Y = \overline{T} \bullet \overline{S}$ $Z = T + S$		**T:** 0 0 1 1 **S:** 0 1 0 1 **Y:** 1 0 0 0 **Z:** 0 1 1 1	if T is Low (0) *AND* S is Low (0), then Y is Open (1) else Y is Ground (0), Z is the complement of Y.
$Y = \overline{\overline{T} + S}$ $Z = T + S$			if T is High (1) *OR* S is High (1), then Y is Ground (0) else Y is Open (1), Z is the complement of Y.

Figure 2.2.1.3-G

Inputs		T Output (Channel 1): 1 = High-Z (Open), 0 = Low (Ground)									
		1	2	3	4	5	6	7	8	B	N
A	B	A•B	A•$\overline{B}$	$\overline{A}$•B	$\overline{A•B}$ $\overline{A+B}$	A+B	A+$\overline{B}$	$\overline{A}$+B	$\overline{A+B}$ $\overline{A•B}$	Buffer T=A	Inverter T=$\overline{A}$
0	0	0	0	0	**1**	**0**	1	1	1	0	1
0	1	0	0	**1**	0	1	**0**	1	1	0	1
1	0	0	**1**	0	0	1	1	**0**	1	1	0
1	1	**1**	0	0	0	1	1	1	**0**	1	0

Inputs		S Output (Channel 2): 1 = High-Z (Open), 0 = Low (Ground)									
		1	2	3	4	5	6	7	8	B	N
C	D	C•D	C•$\overline{D}$	$\overline{C}$•D	$\overline{C•D}$ $\overline{C+D}$	C+D	C+$\overline{D}$	$\overline{C}$+D	$\overline{C+D}$ $\overline{C•D}$	Buffer S=C	Inverter S=$\overline{C}$
0	0	0	0	0	**1**	**0**	1	1	1	0	1
0	1	0	0	**1**	0	1	**0**	1	1	0	1
1	0	0	**1**	0	0	1	1	**0**	1	1	0
1	1	**1**	0	0	0	1	1	1	**0**	1	0

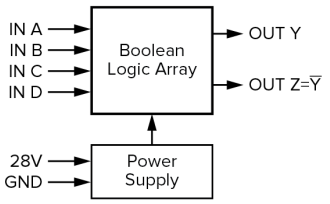
Inputs		Y, Z Output (Gate 3)*			
		N1	N2	N3	N4
		Y=T•$\overline{S}$ Z=$\overline{T}$•S	Y=T•$\overline{S}$	Y=$\overline{T}$•S	Y=$\overline{T}$•$\overline{S}$ Z=T•S
		Y=$\overline{T}$•$\overline{S}$ Z=T+S	Z=T+$\overline{S}$	Z=T+S	Y=$\overline{T+S}$ Z=T+S
T	S	Y , Z	Y , Z	Y , Z	Y , Z
0	0	0 , 1	0 , 1	0 , 1	**1 , 0**
0	1	0 , 1	0 , 1	**1 , 0**	0 , 1
1	0	0 , 1	**1 , 0**	0 , 1	0 , 1
1	1	**1 , 0**	0 , 1	0 , 1	0 , 1

*Outputs: 1 = High-Z (Open), 0 = Low (Ground)

2.2.1.4 Defined Logic 4 (DL4)

The Defined Logic 4 (DL4) is a combinational logic gate device that decodes four inputs to control two orthogonal outputs, see Figure 2.2.1.4-A.

Figure 2.2.1.4-A



Application Performance

The Defined Logic 4 is a digital electronic logic circuit controller that performs Boolean logic gate operations based upon the decode of 4 inputs. The device can perform a 4-bit binary (BNR) or binary-coded decimal (BCD) decode. The device monitors the signal levels of four inputs and holds the state of the two orthogonal outputs until the inputs detect a state change. When the specified decode of Inputs ABCD = *TRUE*, OUT Y is active Open (1), and OUT Z is active Ground (0). Logic gate decodes are defined in the following truth table, see Figure 2.2.1.4-B.

Four-Input Logic Gate Options

NEXSYS Defined Logic components also offer the four-input (ABCD) *AND* operation, as well as *OR* such that one is the binary complement of the other, which produces the two orthogonal outputs (YZ). For example, the four-input (ABCD) *AND* gate operation produces an Active Open (1) OUT (Y) if all inputs are High (1) and the *OR* gate produces an Active Open (1) OUT (Z) if ***one OR more*** of its inputs are High (1). The four-input logic gates are dedicated functions integral to the DL4 component, and has 16 variations.

Figure 2.2.1.4-B

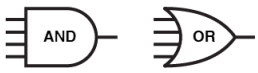
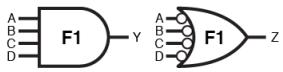
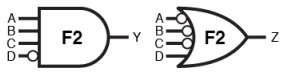
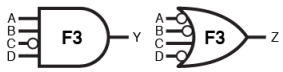
Four-Input Combination Gate Symbols		Combinational Gate Expression	
		The four input *AND* gate produces an Active Open (1) Y Output only if all inputs are High (1). The four input, combination *OR* gate (Z) is the complement of Y.	
Equation	**Variation**	**TRUTH TABLE**	**Boolean Logic "if" Statement**
$Y = A \cdot B \cdot C \cdot D$ $Z = \overline{A} + \overline{B} + \overline{C} + \overline{D}$		**A:** 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 **B:** 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 **C:** 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 **D:** 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 **Y:** 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 **Z:** 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	if A *AND* B *AND* C *AND* D is High (1), then Y is Open (1), else Y is Ground (0), Z is the complement of Y.
$Y = A \cdot B \cdot C \cdot \overline{D}$ $Z = \overline{A} + \overline{B} + \overline{C} + D$		**A:** 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 **B:** 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 **C:** 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 **D:** 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 **Y:** 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 **Z:** 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1	if A *AND* B *AND* C is High (1), when D is Low (0), then Y is Open (1), else Y is Ground (0), Z is the complement of Y.
$Y = A \cdot B \cdot \overline{C} \cdot D$ $Z = \overline{A} + \overline{B} + C + \overline{D}$		**A:** 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 **B:** 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 **C:** 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 **D:** 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 **Y:** 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 **Z:** 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1	if A *AND* B *AND* D is High (1), when C is Low (0) then, Y is Open (1), else Y is Ground (0), Z is the complement of Y.

Figure 2.2.1.4-B

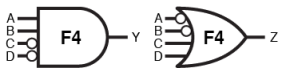
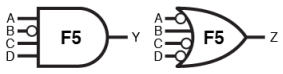
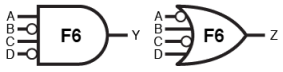
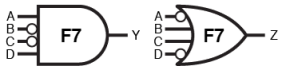
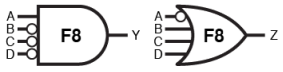
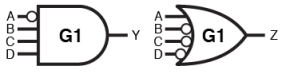
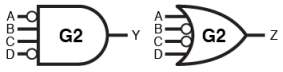
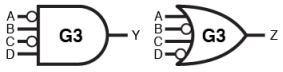
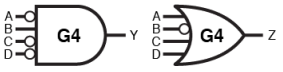
$Y = A \cdot B \cdot \overline{C} \cdot \overline{D}$ $Z = \overline{A} + \overline{B} + C + D$		**A:** 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 **B:** 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 **C:** 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 **D:** 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 **Y:** 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 **Z:** 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1	if A *AND* B is High (1), when C *AND* D is Low (0), then Y is Open (1), else Y is Ground (0), Z is the complement of Y.
$Y = A \cdot \overline{B} \cdot C \cdot D$ $Z = \overline{A} + B + \overline{C} + \overline{D}$		**A:** 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 **B:** 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 **C:** 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 **D:** 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 **Y:** 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 **Z:** 1 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1	if A *AND* C *AND* D is High (1), when B is Low (0) then, Y is Open (1), else Y is Ground (0), Z is the complement of Y.
$Y = A \cdot \overline{B} \cdot C \cdot \overline{D}$ $Z = \overline{A} + B + \overline{C} + D$		**A:** 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 **B:** 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 **C:** 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 **D:** 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 **Y:** 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 **Z:** 1 1 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1	if A AND C is High (1), when B AND D is Low (0), then Y is Open (1), else Y is Ground (0), Z is the complement of Y.
$Y = A \cdot \overline{B} \cdot \overline{C} \cdot D$ $Z = \overline{A} + B + C + \overline{D}$		**A:** 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 **B:** 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 **C:** 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 **D:** 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 **Y:** 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 **Z:** 1 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1	if A *AND* D is High (1), when B *AND* C is Low (0), then Y is Open (1), else Y is Ground (0), Z is the complement of Y.
$Y = A \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$ $Z = \overline{A} + B + C + D$		**A:** 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 **B:** 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 **C:** 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 **D:** 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 **Y:** 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 **Z:** 1 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1	if A is High (1), when B *AND* C *AND* D is Low (0), then Y is Open (,1) else Y is Ground (0), Z is the complement of Y.
$Y = \overline{A} \cdot B \cdot C \cdot D$ $Z = A + \overline{B} + \overline{C} + \overline{D}$		**A:** 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 **B:** 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 **C:** 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 **D:** 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 **Y:** 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 **Z:** 1 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1	if B *AND* C *AND* D is High (1), when A is Low (0) then, Y is Open (1), else Y is Ground (0), Z is the complement of Y.
$Y = \overline{A} \cdot B \cdot C \cdot \overline{D}$ $Z = A + \overline{B} + \overline{C} + D$		**A:** 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 **B:** 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 **C:** 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 **D:** 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 **Y:** 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 **Z:** 1 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1	if B *AND* C High (1), when A *AND* D is Low (0), then Y is Open (1), else Y is Ground (0), Z is the complement of Y.
$Y = \overline{A} \cdot B \cdot \overline{C} \cdot D$ $Z = A + \overline{B} + C + \overline{D}$		**A:** 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 **B:** 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 **C:** 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 **D:** 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 **Y:** 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 **Z:** 1 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1	if B *AND* D is High (1), when A *AND* C is Low (0), then Y is Open (1), else Y is Ground (0), Z is the complement of Y.
$Y = \overline{A} \cdot B \cdot \overline{C} \cdot \overline{D}$ $Z = A + \overline{B} + C + D$		**A:** 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 **B:** 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 **C:** 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 **D:** 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 **Y:** 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 **Z:** 1 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1	if B is High (1), when A *AND* C *AND* D is Low (0), then Y is Open (,1) else Y is Ground (0), Z is the complement of Y.

Figure 2.2.1.4-B

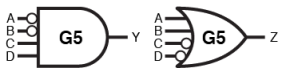
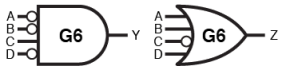
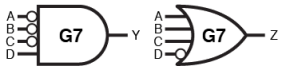
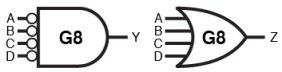
$Y = \overline{A} \cdot \overline{B} \cdot C \cdot D$ $Z = A + B + \overline{C} + \overline{D}$		**A:** 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 **B:** 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 **C:** 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 **D:** 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 **Y:** 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 **Z:** 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1	if C *AND* D is High (1), when A *AND* B is Low (0), then Y is Open (1), else Y is Ground (0), Z is the complement of Y.
$Y = \overline{A} \cdot \overline{B} \cdot C \cdot \overline{D}$ $Z = A + B + \overline{C} + D$		**A:** 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 **B:** 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 **C:** 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 **D:** 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 **Y:** 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 **Z:** 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1	if C is High (1), when A *AND* B *AND* D is Low (0), then Y is Open (1,) else Y is Ground (0), Z is the complement of Y.
$Y = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot D$ $Z = A + B + C + \overline{D}$		**A:** 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 **B:** 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 **C:** 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 **D:** 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 **Y:** 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 **Z:** 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1	if D is High (1), when A *AND* B *AND* C is Low (0), then Y is Open (1,) else Y is Ground (0), Z is the complement of Y.
$Y = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$ $Z = A + B + C + D$		**A:** 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 **B:** 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 **C:** 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 **D:** 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 **Y:** 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 **Z:** 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	if A *AND* B *AND* C *AND* D is Low (0), then Y is Open (1), else Y is Ground (0), Z is the complement of Y.

Figure 2.2.1.4-C

Inputs				F1	F2	F3	F4	F5	F6	F7	F8	G1	G2	G3	G4	G5	G6	G7	G8
				$Y=A\cdot B\cdot C\cdot D$	$Y=A\cdot B\cdot C\cdot \overline{D}$	$Y=A\cdot B\cdot \overline{C}\cdot D$	$Y=A\cdot B\cdot \overline{C}\cdot \overline{D}$	$Y=A\cdot \overline{B}\cdot C\cdot D$	$Y=A\cdot \overline{B}\cdot C\cdot \overline{D}$	$Y=A\cdot \overline{B}\cdot \overline{C}\cdot D$	$Y=A\cdot \overline{B}\cdot \overline{C}\cdot \overline{D}$	$Y=\overline{A}\cdot B\cdot C\cdot D$	$Y=\overline{A}\cdot B\cdot C\cdot \overline{D}$	$Y=\overline{A}\cdot B\cdot \overline{C}\cdot D$	$Y=\overline{A}\cdot B\cdot \overline{C}\cdot \overline{D}$	$Y=\overline{A}\cdot \overline{B}\cdot C\cdot D$	$Y=\overline{A}\cdot \overline{B}\cdot C\cdot \overline{D}$	$Y=\overline{A}\cdot \overline{B}\cdot \overline{C}\cdot D$	$Y=\overline{A}\cdot \overline{B}\cdot \overline{C}\cdot \overline{D}$
				$Z=\overline{A}+\overline{B}+\overline{C}+\overline{D}$	$Z=\overline{A}+\overline{B}+\overline{C}+D$	$Z=\overline{A}+\overline{B}+C+\overline{D}$	$Z=\overline{A}+\overline{B}+C+D$	$Z=\overline{A}+B+\overline{C}+\overline{D}$	$Z=\overline{A}+B+\overline{C}+D$	$Z=\overline{A}+B+C+\overline{D}$	$Z=\overline{A}+B+C+D$	$Z=A+\overline{B}+\overline{C}+\overline{D}$	$Z=A+\overline{B}+\overline{C}+D$	$Z=A+\overline{B}+C+\overline{D}$	$Z=A+\overline{B}+C+D$	$Z=A+B+\overline{C}+\overline{D}$	$Z=A+B+\overline{C}+D$	$Z=A+B+C+\overline{D}$	$Z=A+B+C+D$
				Outputs: 1 = High-Z (Open), 0 = Low (Ground)															
A	B	C	D	Y , Z	Y , Z	Y , Z	Y , Z	Y , Z	Y , Z	Y , Z	Y , Z	Y , Z	Y , Z	Y , Z	Y , Z	Y , Z	Y , Z	Y , Z	Y , Z
0	0	0	0	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	**1 , 0**
0	0	0	1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	**1 , 0**	0 , 1
0	0	1	0	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	**1 , 0**	0 , 1	0 , 1
0	0	1	1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	**1 , 0**	0 , 1	0 , 1	0 , 1
0	1	0	0	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	**1 , 0**	0 , 1	0 , 1	0 , 1	0 , 1
0	1	0	1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	**1 , 0**	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1
0	1	1	0	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	**1 , 0**	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1
0	1	1	1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	**1 , 0**	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1
1	0	0	0	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	**1 , 0**	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1
1	0	0	1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	**1 , 0**	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1
1	0	1	0	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	**1 , 0**	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1
1	0	1	1	0 , 1	0 , 1	0 , 1	0 , 1	**1 , 0**	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1
1	1	0	0	0 , 1	0 , 1	0 , 1	**1 , 0**	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1
1	1	0	1	0 , 1	0 , 1	**1 , 0**	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1
1	1	1	0	0 , 1	**1 , 0**	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1
1	1	1	1	**1 , 0**	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1	0 , 1

2.2.1.5 Defined Logic, Operating Parameters

Figure 2.2.1.5-A	
Description	Parameters
Operating Parameters	
Operating Voltage (Max. / Nom. / Min.)	+32 VDC / +28 VDC / +18 VDC
Power Supply Input Current	4 mA (Maximum)
Reset From Power Loss at 25°C	5 sec (Minimum) at +25° C
Hold Up On Power Loss at 25°C	200 ms (Minimum)
Input Parameters	
Propagation Timing A, B, C & D to output at 25°C	Low to High 20 ms (Maximum) High to Low 80 ms (Maximum)
* High Level Input Voltage (V_{IH}) at 25°C	+4 VDC (Minimum)
* Low Level Input Voltage (V_{IL}) at 25°C	+1.2 VDC (Maximum)
Low Level Input Current (I_{IL}) at 25°C	1mA (Maximum)
All Pulled-up inputs are diode isolated	
Output Parameters	
Output Load Capacity	2.0 A (Resistive) / 1.0 A (Motor) / 0.8 A (Inductive/Lamp)
On-State Resistance at 25°C	Typical 0.07 ohms / Maximum 0.09 ohms
Off-State Resistance at 25°C	Open Drain (High-Z), Fuse-Protected MOSFET, +32 VDC Maximum
Temperature	
Operating & Non-Operating	-55° C to +85° C
Reliability MIL-HDBK-217F, Notice 2	
Airborne Inhabited Cargo (AIC) at 40° C Continuous Operation	MTBF = 131,574 hrs
** V_{IL} and V_{IH} specifications are in reference to unit Ground.*	

For Qualification Summary, see Appendix A

2.2.2 Solid State Relay

Summary Description

NEXSYS Solid State Relays are available individually (SSR), Series A (4 Pin), or in a combination of four (SSRCH), Series C (8 Pin), see Figure 2.2.2.0-A and Figure 2.2.2.0-B. The Solid-State Relays perform custom digital and analog signal control, as well as audio and data signal switching. The broad operating voltage range affords use in numerous applications from simple polarity reversal to logic gate functions like AND, OR, and BUFFER. The Solid-State Relays perform similar functions to a stand-alone mechanical relay without the challenges of external packaging. While Solid State Relays include the advantages of a solid-state design with opto-isolation, high reliability, and low power consumption.

The Solid State Relays feature an integrated electronic circuit to perform signal buffering, optical isolation, and surge-suppression between inputs and outputs, eliminating possible sneak paths. The NEXSYS Solid State Relay (SSR1, SSR2, SSR3, SSRC) is a commercial-off-the-shelf (COTS) item. This standard catalog hardware includes features to allow for flexible interface design solutions while also meeting aircraft performance standards. The SSR is designed, tested, and qualified to MIL-PRF-22885/116, MIL-PRF-22885/117, DO-160 and MIL-STD-461 requirements. Specifications are available in our MIL-PRF and DO-160 Documents page, and the qualification table is available in Appendix A.

Figure 2.2.2.0-A

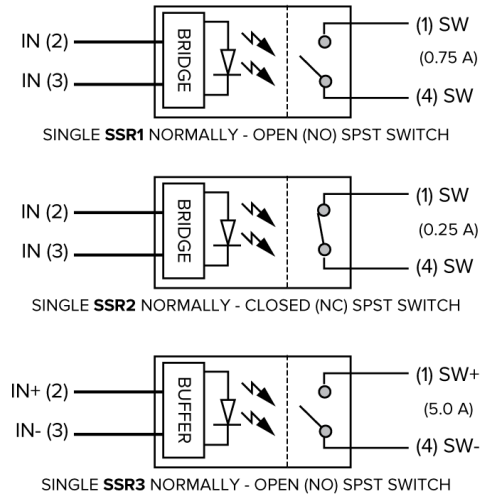
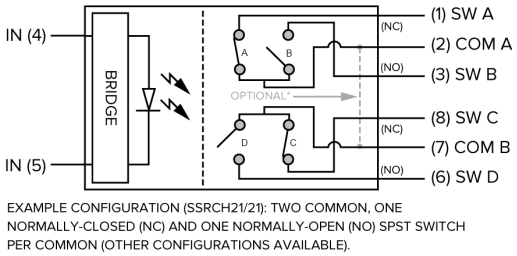


Figure 2.2.2.0-B



**Single common option when specified*

Input Characteristics

NEXSYS Solid State Relays have two control bridge types. The SSR1, SSR2, and SSRC have a bidirectional control bridge which allows DC voltages to be applied in either direction for polarity insensitive design flexibility. The SSR3H has a unidirectional control buffer, which is ideal for applications where current flow is only required in one direction. The SSR3H input circuitry is diode isolated and buffered for reliable operation. The SSRs are available in multiple operating voltages for custom switching control, as indicated below. See additional sections for specific details concerning the Input/Output (I/O) interface.

IN (PIN 2, 3), Single SSR1 and SSR2: High (H) 28V (Nom.), 6.3 mA (Nom.); Mid (M) 14V (Nom.), 6.2 mA (Nom.); and Low (L) 5V (Nom.), 12.1 mA (Nom.).

IN (PIN 2, 3), Single SSR3H: High (H) 28V (Nom.), 10 mA (Nom.), 8V (Min.), 7 mA (Nom.).
Note: PIN 2 and 3 are polarity sensitive. PIN 2 is for (+) input and PIN 3 is for (-) input.

IN (PIN 4, 5), Combination SSR: High (H) 28V (Nom.) 25 mA (Max).

Output Characteristics

NEXSYS Solid State Relays feature isolated Switch (SW) outputs to perform functions that may originate from remote inputs or switch closures. Solid State Relay switch outputs are fused and surge-protected against transients and overload conditions, see Figure 2.2.2.3-A (Operating Parameters) for electrical load rating types.

SW (PIN 1, 4), Single SSR1 and SSR2: SPST, Normally-Open (SSR1), and Normally-Closed (SSR2).

SW (PIN 1, 4), Single SSR3H: SPST, Normally-Open (NO). PIN 1 and 4 are polarity sensitive. PIN 1 is for (+) input and PIN 4 is for (-) input. DC Voltage only.

SW/COM (PIN 1, 2, 3, 8, 7, 6), Combination SSRCH: Four SPST, Normally-Open (1) and Normally-Closed (2).

Configuration Options

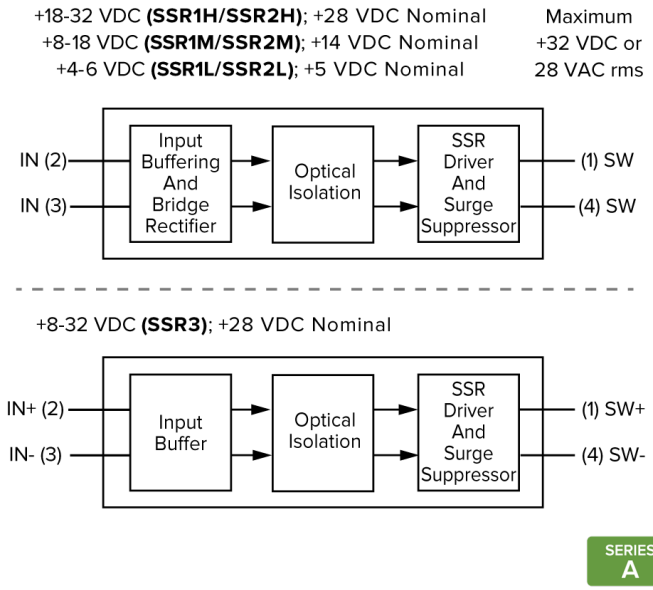
NEXSYS Solid State Relays are specified individually (SSR), or in a combination of four (SSRCH). The SSRCH configuration is internally connected to reduce external splices and to perform synchronized switching. SSRs power-up in a known state, either Normally-Open (SSR1 & SSR3H) or Normally-Closed (SSR2). With operating voltage applied across the inputs, the Normally-Open (NO) SPST switch closes to conduct the connected signal, and the Normally-Closed (NC) SPST switch opens. The following configuration options are available for Single (SSR) SSRs, including SSR1, SSR2, and SSR3H.

2.2.2.1 Single (SSR)

Single SSR: Series A (4 Pin) single SSRs are available in Normally-Open (SSR1 & SSR3H) and Normally-Closed (SSR2) versions. SSR1 and SSR2 have three nominal input voltage options; Low (+5 VDC), Mid (+14 VDC), and High (+28 VDC). SSR3H is exclusively available with a nominal input voltage of +28 VDC.

The current draw of the three voltage options for SSR1 and SSR2 is 12.1 mA (+5 VDC), 6.2 mA (+14 VDC), and 6.3 mA (+28 VDC), see Figure 2.2.2.1-A. The current draw for SSR3H is 10 mA (+28 VDC).

Figure 2.2.2.1-A



Normally Open (NO): 0.75 A (Resistive) max output load capacity*

SSR1H: Normally-Open (NO) SPST Closes when +18 to 32 VDC is applied across the inputs.
SSR1M: Normally-Open (NO) SPST Closes when +8 to 18 VDC is applied across the inputs.
SSR1L: Normally-Open (NO) SPST Closes when +4 to 6 VDC is applied across the inputs.

Normally Closed (NC): 0.25 A (Resistive) maximum output load capacity*

SSR2H: Normally-Closed (NC) SPST Opens when +18 to 32 VDC is applied across the inputs.
SSR2M: Normally-Closed (NC) SPST Opens when +8 to 18 VDC is applied across the inputs.
SSR2L: Normally-Closed (NC) SPST Opens when +4 to 6 VDC is applied across the inputs.

High Current Normally Open (NO): 5 A (Resistive) maximum output load capacity**

SSR3H: Normally-Open (NO) SPST Closes when +8 to +32 VDC is applied across the IN+ and IN- inputs.

**The outputs switch up to +32 VDC or 28 VAC (V_{RMS}) and are surge-protected against transients and overload conditions via a Very Fast Acting fuse.*

***The output switches up to +32 VDC and is surge-protected against transients and overload conditions via a Very Fast Acting fuse.*

Signal Description

For a description of the input and output functions of the Single SSR (SSR1 & SSR2) component, see Figure 2.2.2.1-B (SSR3H) see Figure 2.2.2.1-C.

Figure 2.2.2.1-B

Signals	Pins	Normally Open (NO) Logic Functions SSR1H, SSR1M & SSR1L	Normally Closed (NC) Logic Functions SSR2H, SSR2M & SSR2L	Comments
IN	2 & 3	Input: Active when DC voltage applied across PINS 2 and 3.		DC Voltage can be applied in either direction. *See Note 1.*
SW	1 & 4	Output: Conductive between pins 1 and 4 in either polarity when Input is active. Output is high impedance when input is off.	Output: High impedance between pins 1 and 4 when Input is active. Output is conductive in either polarity when input is off.	Approx. 0.5 volt drop at 0.75 A load between pins 1 and 4 when conducting. *See Note 2.*

Notes

1. *Due to bidirectional nature of bridge, external diode isolation is recommended on either PIN 2 or 3 if unidirectional operation is required.*
2. *Output SW (PINS 1 & 4) is fused at 1.6 A (SSR1) and 0.5 A (SSR2) to protect against transients and overload conditions.*

Figure 2.2.2.1-C

Signals	Pins	Normally Open (NO) Logic Functions SSR3H	Comments
IN +	2	Input: Active when positive DC voltage applied across PINS 2 and 3.	DC Voltage only +32 VDC Max
IN -	3		
OUT +	1	Output: Conductive from pins 1 and 4 when Input is active.	Output is polarity sensitive. Applying current in the reverse direction can destroy the output driver.
OUT -	4		

Notes

1. *Output is fused at 8A for output overload conditions.*

2.2.2.2 Combination (SSRC)

Combination SSRCH: The output load capacity ratings of the Normally-Open (NO) and Normally-Closed (NC) SSRCH configurations and the switch logic performs identically to the Single SSR. However, the internal connections differ in three switching options with multiple combinations of NO (denoted by a 1) and NC (denoted by a 2) switch contacts; see Figure 2.2.2.2-A, Figure 2.2.2.2-C, and Figure 2.2.2.2-E. The most common configurations are listed below in the tables in bold text; see Figure 2.2.2.2-B, Figure 2.2.2.2-D, and Figure 2.2.2.2-F.

Four Switch, Single Common: Four (4) SPST contacts, configured with a single, internally spliced common, see Figure 2.2.2.2-A and Figure 2.2.2.2-B.

Figure 2.2.2.2-A

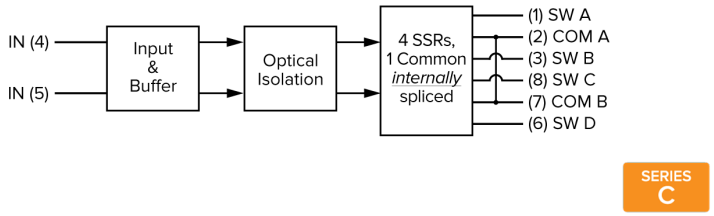


Figure 2.2.2.2-B

Configuration (SSRCH/ABCD)	Common A & B, **internally** spliced
SSRCH/1111	**4 NO SPST**
SSRCH/2222	**4 NC SPST**
SSRCH/1122	**2 NO and 2 NC SPST, grouped**
SSRCH/1212	**2 NO and 2 NC SPST, collated**
SSRCH/2121	**2 NC SPST and 2 NO SPST, collated**
SSRCH/1112	3 NO SPST, grouped and 1 NC SPST
SSRCH/1121	1 NC SPST between 3 NO SPST
SSRCH/1211	1 NC SPST between 3 NO SPST
SSRCH/1221	2 NO SPST, split and 2 NC SPST, grouped
SSRCH/1222	1 NO SPSTand 3 NC SPST, grouped
SSRCH/2111	1 NC SPSTand 3 NO SPST, grouped
SSRCH/2112	2 NC SPST, split and 2 NO SPST, grouped
SSRCH/2122	1 NO SPSTbetween 3 NC SPST
SSRCH/2211	2 NC SPST and 2 NO SPST, grouped
SSRCH/2212	1 NO SPSTbetween 3 NC SPST
SSRCH/2221	3 NC SPST, grouped and 1 NO SPST

Dual Switch Pair: Four (4) SPST contacts (two pairs), configured with a single, internally spliced common per pair, see Figure 2.2.2.2-C and Figure 2.2.2.2-D.

Figure 2.2.2.2-C

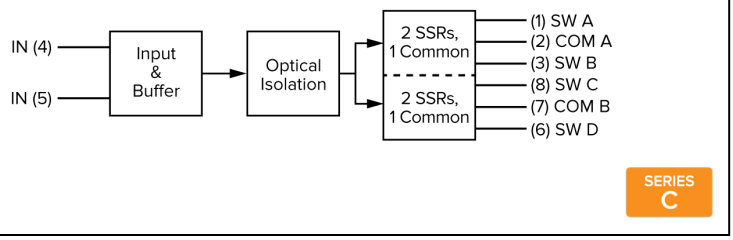


Figure 2.2.2.2-D

Configuration (SSRCH/AB/CD)	Common A	Common B
SSRCH/11/11	**2 NO SPST**	**2 NO SPST**
SSRCH/11/22	**2 NO SPST**	**2 NC SPST**
SSRCH/12/12	**1 NO, 1 NC SPST**	**1 NO, 1 NC SPST**
SSRCH/22/22	**2 NC SPST**	**2 NC SPST**
SSRCH/21/21	**1 NC SPST and 1 NO SPST**	**1 NC SPST and 1 NO SPST**
SSRCH/11/12	2 NO SPST	1 NO SPST and 1 NC SPST
SSRCH/11/21	2 NO SPST	1 NC SPST and 1 NO SPST
SSRCH/12/11	1 NO SPST and 1 NC SPST	2 NO SPST
SSRCH/12/21	1 NO SPST and 1 NC SPST	1 NO SPST and 1 NC SPST
SSRCH/12/22	1 NO SPST and 1 NC SPST	2 NC SPST
SSRCH/21/11	1 NC SPST and 1 NO SPST	2 NO SPST
SSRCH/21/12	1 NC SPST and 1 NO SPST	1 NO SPST and 1 NC SPST
SSRCH/21/22	1 NC SPST and 1 NO SPST	2 NC SPST
SSRCH/22/11	2 NC SPST	2 NO SPST
SSRCH/22/12	2 NC SPST	1 NO SPST and 1 NC SPST
SSRCH/22/21	2 NC SPST	1 NC SPST and 1 NO SPST

Three Switch, Single Common, One Switch Single Common: Three (3) SPST contacts configured with a single, internally spliced common and one (1) SPST contact, configured with a single, internally spliced common, see Figure 2.2.2.2-E and Figure 2.2.2.2-F.

Figure 2.2.2.2-E

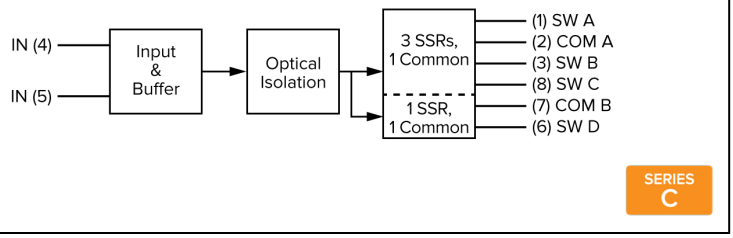


Figure 2.2.2.2-F

Configuration (SSRCH/ABC/D)	Common A	Common B
SSRCH/111/2	**3 NO SPST**	**1 NC SPST**
SSRCH/222/1	**3 NC SPST**	**1 NO SPST**
SSRCH/111/1	3 NO SPST	1 NO SPST
SSRCH/112/1	2 NO SPST, grouped and 1 NC SPST	1 NO SPST
SSRCH/112/2	2 NO SPST, grouped and 1 NC SPST	1 NC SPST
SSRCH/121/1	2 NO SPST, split and 1 NC SPST	1 NO SPST
SSRCH/121/2	2 NO SPST, split and 1 NC SPST	1 NC SPST
SSRCH/122/1	1 NO SPST and 2 NC SPST, grouped	1 NO SPST
SSRCH/122/2	1 NO SPST and 2 NC SPST, grouped	1 NC SPST
SSRCH/211/1	1 NC SPST and 2 NO SPST, grouped	1 NO SPST
SSRCH/211/2	1 NC SPST and 2 NO SPST, grouped	1 NC SPST
SSRCH/212/1	2 NC SPST, split and 1 NC SPST	1 NO SPST
SSRCH/212/2	2 NC SPST, split and 1 NC SPST	1 NC SPST
SSRCH/221/1	2 NC SPST, grouped and 1 NO SPST	1 NO SPST
SSRCH/221/2	2 NC SPST, grouped and 1 NO SPST	1 NC SPST
SSRCH/222/2	3 NC SPST	1 NC SPST

Signal Description

For a description of the input and output functions of the Combination SSR (SSRCH) component, see Figure 2.2.2.2-G.

Figure 2.2.2.2-G

Signals	Pins	Logic Functions Normally Open (1)*	Logic Functions Normally Closed (2)**
A, B, C, and D	1 (A), 3 (B), 8 (C), 6 (D)	Shorted to Common A or B when the inputs (IN) are Active	Shorted to Common A or B when the inputs (IN) are not Active
Common	2 (COM A) 7 (COM B)	Signal Common A and B	
IN	4 & 5	Active when +28 VDC is applied across the inputs (IN)	

Notes

1. *Due to bidirectional nature of bridge, external diode isolation is recommended on either (IN) if unidirectional operation is required.*
2. *Outputs (A,B,C, and D) fused at 1.6 A* and 0.5 A** to protect against transients and overload conditions.*
3. *The internally splice common (PINS 2 and 7) of the Four Switch, Single Common configuration is rated at 1.5 A.*

** 1 = Normally Open (NO) SSR ** 2 = Normally Closed (NC) SSR*

2.2.2.3 Solid State Relay, Operating Parameters

Figure 2.2.2.3-A

Description	Parameters (SSR1 and SSR2)			SSR3H
	+28 VDC Input	**+14 VDC Input**	**+5 VDC Input**	**+28 VDC Input**
Input/Output Parameters				
Maximum Voltage On	+32 VDC	+18 VDC	+6 VDC	+32 VDC
Nominal Voltage On	+28 VDC	+14 VDC	+5VDC	+28 VDC
Minimum Voltage On	+18 VDC	+8 VDC	+4 VDC	+8 VDC
Voltage Off (Maximum)	+6 VDC	+4 VDC	+2 VDC	+1.5 VDC
Typical Operation Current	6.3 mA (SSR1 /SSR2) 25 mA (SSRCH)	6.2 mA	12.1 mA	10 mA
Typical Input Impedance at 25°C	4,444 ohms (SSR1 / SSR2) 1,111 ohms (SSRCH)	2,258 ohms	413 ohms	2800 ohms
Turn On Time Maximum at 25°C	3 ms	3 ms	5 ms	0.15 ms
Turn Off Time Maximum at 25°C	0.5 ms	0.5 ms	0.5 ms	0.4 ms
Maximum Output Voltage	+32 VDC or 28 VAC (V_{RMS})			
Minimum Output Voltage	N/A			

	SSR1H, SSR1M and SSR1L (NO)	**SSR2H, SSR2M and SSR2L (NC)**	**SSR3H**
Output Parameters			
Resistive	0.75 A	0.25 A	5.0 A
Inductive	0.5 A (300 mH)	0.25 A (300 mH)	5.0 A
Lamp	0.1 A (1 A, 10 ms. inrush)	N/A	N/A
Audio	< 600 ohms		N/A
On-State Resistance at 25°C	Typical 0.2 ohms AC/DC Maximum 0.25 ohms	Typical 1.6 ohms AC/DC Maximum 3.1 ohms	Typical 0.3 ohms
Off-State Resistance at 25°C	Open Drain (High-Z), Fuse-Protected MOSFET, +32 VDC Maximum	Open Drain (High-Z), Fuse-Protected MOSFET, +32 VDC Maximum	Open Drain (High Z), Fuse-Protected MOSFET, +32 VDC Maximum
Temperature			
Operating	-55°C to +85°C		
Non-Operating	-55°C to +85°C		
Reliability MIL-HDBK-217F, Notice 2			
Airborne Inhabited Cargo (AIC) at +40°C Continuous Operation	MTBF = 668,509 hrs		MTBF = 921,919 hrs

**NO (1) and NC (2) Output Load Capacity should be considered when packaged in the same housing.*

For Qualification Summary, see Appendix A

2.3 State Control Components

Components that use digital electronic latching circuitry to control and store either a single or a series of output states.

State Control components include:

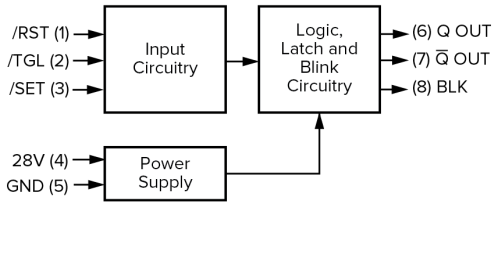
- Electronic Latch
- Electronic Rotary

2.3.1 Electronic Latch

Summary Description

The NEXSYS Electronic Latch (EL1, EL2) is a Series C (8 Pin) electronic component with multiple trigger modes that activate orthogonal switching (flip-flop) between two known states, see Figure 2.3.1.0-A. The device can perform similar functions of traditional electromagnetic or solenoid switches but at a fraction of the size, weight, and power requirements due to its solid-state design.

Figure 2.3.1.0-A



The NEXSYS Electronic Latch (EL1, EL2) is a commercial-off-the-shelf (COTS) item. This standard catalog hardware includes features to allow for flexible interface design solutions while also meeting aircraft performance standards. The EL is designed, tested, and qualified to MIL-PRF-22885/116, MIL-PRF-22885/117, DO-160 and MIL-STD-461 requirements. Specifications are available in our MIL-PRF and DO-160 Documents page, and the qualification table is available in Appendix A.

Input Characteristics

The NEXSYS Electronic Latch inputs are Power (28V), Ground (GND), Toggle (/TGL), Set (/SET), and Reset (/RST). The Signal Definition Table and Truth Table provide specific details concerning the Input/Output (I/O) interface, see Figure 2.3.1.0-B and Figure 2.3.1.0-C. The inputs include the following characteristics for custom switching and output control. Electronic Latch input circuity is diode isolated, buffered, and debounced for reliable operation.

28V (PIN 4): Operating Voltage (Nom.), Current Draw 4 mA (Max).
GND (PIN 5): Continuous Ground required, otherwise, inadvertent operation could occur.
/TGL (PIN 2): Detects High to Low signal transitions, which function as the control interface to drive outputs.
/SET (PIN 3): Immediate activation to the Set state.
/RST (PIN 1): Immediate activation to the Reset state.

Output Characteristics

The NEXSYS Electronic Latch features conditioned outputs Q, $\overline{Q}$ and Blink (BLK) to perform functions that may originate from remote inputs or switch closures. All outputs are open-drain High-Z (Open) when not active, fused, and surge-protected against transients and overload conditions. The output load capacity is 2.0 A , see Figure 2.3.1.1-A (Operating Parameters) for electrical load rating types.

Q (PIN 6), $\overline{Q}$ (PIN 7): Active = Low (Ground), Not Active = High-Z (Open) and $\overline{Q}$ is the complement of Q.
BLK (PIN 8): 1 Hz square wave (50% duty cycle) oscillation frequency (Blink), alternating High-Z (Open) to Low (Ground).

Configuration Options

The NEXSYS Electronic Latch is available in two configurations for custom solid-state switching control. The device powers-up in a specified, known state. Upon power-up, High to Low (⎍)signal transitions to the /SET, /TGL, and /RST input functions to control the Q, $\overline{Q}$ and BLK outputs.

Electronic Latch 1 (EL1), Default Power-Up State: Q = High-Z (Open), $\overline{Q}$ = Low (Ground) and BLK = High-Z (Open).

Electronic Latch 2 (EL2), Default Power-Up State: Q = Low (Ground), $\overline{Q}$ = High-Z (Open) and BLK = 1 Hz oscillation frequency.

Signal Description

For a description of the input and output functions of the Electronic Latch component, see Figure 2.3.1.0-B.

Figure 2.3.1.0-B

Pin Reference	Pin Identification	Function	Input Trigger	Description
1	/RST	Input	Low (Ground)	Forces Q OUT to OFF High-Z (Open). Forces $\overline{Q}$ OUT to ON Low (Ground). Forces BLK to Steady ON Low (Ground). See Note 1.
2	/TGL	Input	↓ See Note 4	Toggles Q OUT and $\overline{Q}$ OUT. Toggles blink mode. See Note 2.
3	/SET	Input	Low (Ground)	Forces Q OUT to ON Low (Ground). Forces $\overline{Q}$ OUT to OFF High-Z (Open). Initiates the 1Hz blink mode to BLK Output.
4	28V	Power	–	Power (+18 VDC to +32 VDC)
5	GND	Common	–	Continuous Ground Required.
Pin Reference	**Pin Identification**	**Function**	**Output Active State**	**Description**
6	Q OUT	Output	Low (Ground)	Open Drain Output. Forced OFF High-Z (Open) by /RST Input. Forced ON Low (Ground) by /SET Input. Toggled by Falling Edge of /TGL Input.
7	$\overline{Q}$ OUT	Output	Low (Ground)	Open Drain Output. Forced ON Low (Ground) by /RST Input. Forced OFF High-Z (Open) by /SET Input. Toggled by Falling Edge of /TGL Input.
8	BLK	Output	Low (Ground)	Open Drain Output. Forced ON Low (Ground) while /RST is held Low (Ground). BLK Active (1 Hz) in /SET and Not Active in /RST.

Truth Table

For a description of the operational states of the Electronic Latch component, see Figure 2.3.1.0-C.

Figure 2.3.1.0-C						
Inputs			**Outputs**			**Comments**
/SET	/RST	/TGL	Q OUT	$\overline{Q}$ OUT	Blink	
High-Z (Open)	Low (Ground)	X	High-Z (Open)	Low (Ground)	Steady ON See Note 1	Represents EL1 Power-Up State
Low (Ground)	High-Z (Open)	X	Low (Ground)	High-Z (Open)	1 Hz Blink See Note 1	Represents EL2 Power-Up State
High-Z (Open)	High-Z (Open)	↘ See Note 4	Opposite State	Opposite State	Change State See Note 2	
Low (Ground)	Low (Ground)	X	Low (Ground) See Note 3	Low (Ground) See Note 3	Steady ON See Note 1	

Notes

1. BLK is steady-state Low (Ground) while /RST is held Low (Ground). BLK Active (1 Hz) in /SET and Not Active in /RST. Upon EL1 Power-Up, /RST is internally held Low (Ground) momentarily, causing BLK to flash.
2. /TGL controls BLK, ON = 1 Hz oscillation (50% duty cycle) and OFF = High-Z (Open). /TGL is overridden when /RST or /SET is held Low (Ground).
3. If /SET and /RST release simultaneously, the device returns to the default power-up state. Otherwise, it functions according to the defined input levels.
4. Transition from High-Z (Open) to Low (Ground) toggles Q and $\overline{Q}$. Input signal level definitions are provided in the Parametric Table, see Figure 2.3.1.1-A.

2.3.1.1 Electronic Latch, Operating Parameters

Figure 2.3.1.1-A	
Description	Parameters
Operating Parameters	
Operating Voltage (Max. / Nom. / Min.)	+32 VDC / +28 VDC / +18 VDC
Power Supply Input Current	4 mA (Maximum)
Reset From Power Loss at 25°C	5 sec (Minimum) at +25° C
Hold Up On Power Loss at 25°C	50 ms (Minimum)
Input Parameters	
EL1: /RST, EL2: /SET at 25°C	120 ms (Minimum)
/TGL at 25°C	45 ms (Minimum)
EL1: /SET, EL2: /RST at 25°C	45 ms (Minimum)
* High Level Input Voltage (V_{IH}) at 25°C	+3 VDC (Minimum)
* Low Level Input Voltage (V_{IL}) at 25°C	+0.4 VDC (Maximum)
Low Level Input Current (I_{IL}) at 25°C	1 mA (Maximum)
Note: All signal inputs are diode isolated	
Output Parameters	
Output Load Capacity	2.0 A (Resistive) / 1.0 A (Motor) / 0.8 A (Inductive/Lamp)
On-State Resistance at 25°C	Typical 0.07 ohms / Maximum 0.09 ohms
Off-State Resistance at 25°C	Open Drain (High-Z), Fuse-Protected MOSFET, +32 VDC Maximum
Temperature	
Operating	-55° C to +85° C
Non-Operating	-55° C to +85° C
Reliability MIL-HDBK-217F, Notice 2	
Airborne Inhabited Cargo (AIC) at +40°C Continuous Operation	MTBF = 274,801 hrs
** V_{IL} and V_{IH} specifications are in reference to unit Ground.*	

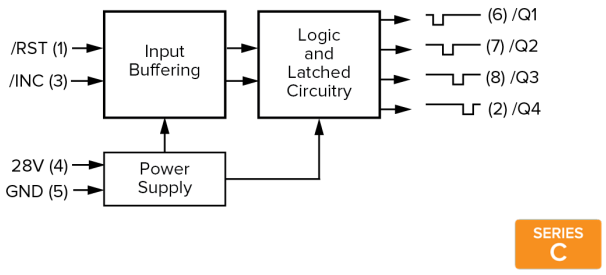
For Qualification Summary, see Appendix A

2.3.2 Electronic Rotary

Summary Description

The NEXSYS Electronic Rotary (ER1) is a Series C (8 Pin) component designed to provide incremental switching through a loop of up to four latched output states (/Q1-/Q4), see Figure 2.3.2.0-A. The product offers a solid-state replacement for applications that traditionally utilize up to a four position rotary device. The NEXSYS Electronic Rotary component provides the ability to use a single illuminated pushbutton switch or indicator to cycle through multiple latched states either from successive switch closures or from a remote source.

Figure 2.3.2.0-A



The NEXSYS Electronic Rotary (ER1) is a commercial-off-the-shelf (COTS) item. This standard catalog hardware includes features to allow for flexible interface design solutions while also meeting aircraft performance standards. The ER is designed, tested, and qualified to MIL-PRF-22885/116, MIL-PRF-22885/117, DO-160 and MIL-STD-461 requirements. Specifications are available in our MIL-PRF and DO-160 Documents page, and the qualification table is available in Appendix A.

Input Characteristics

The NEXSYS Electronic Rotary inputs are Power (28V), Ground (GND), Increment (/INC) and Reset (/RST). Electronic Rotary input circuity is diode isolated, buffered, and debounced for reliable operation. The Signal Description Table and Truth Table provide specific details concerning the Input/Output (I/O) interface, see Figure 2.3.2.0-B and Figure 2.3.2.0-C. The inputs include the following characteristics for custom multi-state switching and output control.

28V (PIN 4): Operating Voltage (Nom.), Current Draw 4 mA (Max).
GND (PIN 5): Continuous Ground required, otherwise, inadvertent operation could occur.
/INC (PIN 3): Detects signal transitions, which function as the control interface to loop through four outputs. /INC is disabled when /RST is held Low (Ground).
/RST (PIN 1): Immediate activation to the /RST state.

Output Characteristics

The NEXSYS Electronic Rotary features conditioned outputs /Q1-/Q4 to perform functions that may originate from remote inputs or switch closures. All outputs are open-drain High-Z (Open) when not active, fused, and surge-protected against transients and overload conditions. The output load capacity is 2.0 A, see Figure 2.3.2.1-A (Operating Parameters) for electrical load rating types.

/Q1 (PIN 6), /Q2 (PIN 7), /Q3 (PIN 8), /Q4 (PIN 2): Active = Low (Ground), Not Active = High-Z (Open).

Configuration Options

The NEXSYS Electronic Rotary standard configuration powers-up in a known state, which is /Q1 = Active Low (Ground) and /Q2-/Q4 = High-Z (Open). Following power-up, /INC will detect a High to Low (⎍) signal transition, and successive transitions will activate the next of four latched outputs in the loop sequence. The ER1 latching circuitry holds the current state until /INC or /RST inputs are toggled, High to Low. Configuring an ER1 circuit to reduce the number of states, advance (skip) a state, hold a state, customize the state sequence or a shift register is performed by a simple input-pin interface.

Reduce State: is performed by wiring the next output state back to /RST. For example, wiring /Q4 to /RST configures a three-state rotary (/Q1-/Q3) circuit.

Advance State: is performed by *NOT* wiring an output. For example, *NOT* wiring /Q1 configures an "OFF" or "STBY" state in /Q1. States /Q2-/Q4 will advance with each successive High to Low transition to /INC, following the *NOT* /Q1 state.

Hold State: is performed by wiring the next output state back to /INC. For example, wiring /Q4 back to /INC configures a hold circuit, until power is cycled.

Custom State: is performed by wiring outputs in a custom sequence. For example, wiring /Q1-/Q4 in a defined sequence configures custom indicator illumination circuit activation (i.e., loop or zigzag).

Shift Register: is performed by wiring ER1 I/O to additional NEXSYS timing and Boolean logic gate components. For example, wiring can be configured with additional NEXSYS components to produce parallel, serial and bidirectional shift register circuits.

Signal Description

For a description of the input and output functions of the Electronic Rotary component, see Figure 2.3.2.0-B.

Figure 2.3.2.0-B

Pin Reference	Pin Identification	Function	Input Trigger
1	/RST	Low (Ground) Resets to State 1 with /Q1 latched Low (Ground) and remains in Reset until Low (Ground) is released.	Low (Ground)
3	/INC	High to Low transition (↘) advances the unit to the next state. Input signal level definitions are provided in the Parametric Table, see Figure 2.3.2.1-A.	Increment input at state 4 will return the unit to state 1
4	28V	Power	+28 VDC
5	GND	Ground	Continuous Ground req'd
Pin Reference	**Pin Identification**	**Function**	**Active State**
6	/Q1	Default upon power-up or Reset is Active Low (Ground).	Active Low (Ground)
7	/Q2	Default upon power-up or Reset is High-Z (Open) and transitions to Active Low (Ground) upon /INC.	Active Low (Ground)
8	/Q3	Default upon power-up or Reset is High-Z (Open) and transitions to Active Low (Ground) upon /INC.	Active Low (Ground)
2	/Q4	Default upon power-up or Reset is High-Z (Open) and transitions to Active Low (Ground) upon /INC.	Active Low (Ground)

Truth Table

For a description of the operational states of the Electronic Rotary component, see Figure 2.3.2.0-C.

Figure 2.3.2.0-C

Inputs			Outputs		
/RST	/INC	/Q1	/Q2	/Q3	/Q4
High	High to Low	Next output, transistions from High-Z (Open) (Open Drain) to Active Low (Ground)			
Low	X	Active Low (Ground)	High-Z (Open) (Open Drain)	High-Z (Open) (Open Drain)	High-Z (Open) (Open Drain)

X = Input has no effect on output, it is a logic don't-care (DC) condition. Note: Only one output is active at any one time.

2.3.2.1 Electronic Rotary, Operating Parameters

Figure 2.3.2.1-A	
Description	Parameters
Operating Parameters	
Operating Voltage (Max. / Nom. / Min.)	+32 VDC / +28 VDC / +18 VDC
Power Supply Input Current	5 mA (Maximum)
Reset From Power Loss at 25°C	5 sec (Minimum) at +25° C
Hold Up On Power Loss at 25°C	200 ms (Minimum)
Input Parameters	
/INC at 25°C	50 ms (Minimum)
/RST at 25°C	80 ms (Minimum)
Timing /INC to output at 25°C	100 ms (Maximum)
* High Level Input Voltage (V_{IH}) at 25°C	+3 VDC (Minimum)
* Low Level Input Voltage (V_{IL}) at 25°C	+1.2 VDC (Maximum)
Low Level Input Current (I_{IL}) at 25°C	1 mA (Maximum)
Note: All signal inputs are diode isolated	
Output Load Capacity	
Output Load Capacity	2.0 A (Resistive) / 1.0 A (Motor) / 0.8 A (Inductive/Lamp)
On-State Resistance at 25°C	Typical 0.07 ohms / Maximum 0.09 ohms
Off-State Resistance at 25°C	Open Drain (High-Z), Fuse-Protected MOSFET, +32 VDC Maximum
Temperature	
Operating	-55° C to +85° C
Non-Operating	-55° C to +85° C
Reliability MIL-HDBK-217F, Notice 2	
Airborne Inhabited Cargo (AIC) at +40°C Continuous Operation	MTBF = 202,483 hrs
** V_{IL} and V_{IH} specifications are in reference to unit Ground.*	

For Qualification Summary, see Appendix A

2.4 Timing Components

Components that detect electronic signal transitions to trigger a time-delayed, pulsed or oscillating output.

Timing components include:

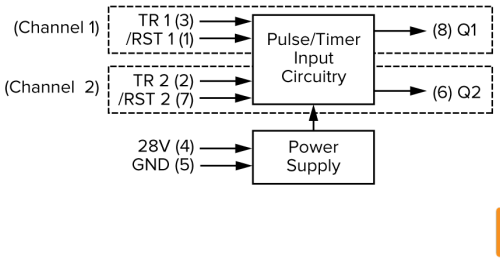
- Pulse/Timer
- Time Delay
- Square Wave Oscillator

2.4.1 Pulse/Timer

Summary Description

The NEXSYS Pulse/Timer (PT1) is a Series C (8 Pin) dual-channel edge detector and pulse generator. Each channel is independent and provides stable retriggerable/resettable one-shot operation for fixed timing applications. The trigger inputs allow unlimited rise and fall transitions that can be specified to sense either a rising-edge (Low to High) or falling-edge (High to Low), see Figure 2.4.1.0-A. Input signal level (edge) definitions are provided in the Parametric Table, see Figure 2.4.1.1-A.

Figure 2.4.1.0-A



The PT1 can generate a wide range of timed pulse widths that are specified as either Active High (High-Z, Open) or Active Low (Ground). The specified time intervals range from 125 ms to 20 sec. Each channel includes a Low-triggered Reset Input (PINS 1, 7) for immediate deactivation of pulsed Outputs, Q1 and Q2 (PINS 8, 6). The channels can be wired in series to provide a propagation delay for a custom, time-delayed one-shot. The PT1 offers a solid-state replacement for electromechanical time delay relays. Other uses include reciprocal transition detection (i.e., “Weight On/Off Wheels”) and limit sensor applications.

The NEXSYS Pulse/Timer (PT1) is a commercial-off-the-shelf (COTS) item. This standard catalog hardware includes features to allow for flexible interface design solutions while also meeting aircraft performance standards. The PT is designed, tested, and qualified to MIL-PRF-22885/116, MIL-PRF-22885/117, DO-160 and MIL-STD-461 requirements. Specifications are available in our MIL-PRF and DO-160 Documents page, and the qualification table is available in Appendix A.

Input Characteristics

The NEXSYS Pulse/Timer inputs are Power (28V), Ground (GND), Trigger 1 (TR 1), Reset 1 (/RST 1), Trigger 2 (TR 2) and Reset 2 (/RST 2). The inputs include the following characteristics for edge detection and timed-output control. Pulse/Timer input circuity is diode isolated, buffered, and debounced for reliable operation. See additional sections for specific details concerning the Input/Output (I/O) interface.

28V (PIN 4): Operating Voltage (Nom.), Current Draw 4 mA (Max).
GND (PIN 5): Continuous Ground required, otherwise, inadvertent operation could occur.
TR 1 (PIN 3), TR 2 (PIN 2): Detect a rising (⌐‾) or falling (‾¬) edge signal level transition, which functions as the control interface trigger to drive timed outputs.
/RST 1 (PIN 1), /RST 2 (PIN 7): Immediate termination (reset) of the pulsed output.

Output Characteristics

The NEXSYS Pulse/Timer features conditioned outputs Channel 1 (Q1) and Channel 2 (Q2) Q to perform functions that may originate from remote inputs or switch closures. All outputs are open-drain High-Z (Open) when not active, fused, and surge-protected against transients and overload conditions. The output load capacity is 2.0 A, see Figure 2.4.1.1-A (Operating Parameters) for electrical load rating types.

Q1 (PIN 8), Q2 (PIN 6): Independent outputs that are one-shot drivers, available in two options. Specified timing options for the output pulse range from 125 ms to 20 seconds.

Configuration Options

The NEXSYS Pulse/Timer offers numerous configurations for custom, solid-state edge-detection and pulsed-output control. The device powers-up in a specified, known state. After power-up, the TR 1 and TR 2 inputs detect signal transitions to control the Q1 and Q2 outputs.

Trigger Options TR 1 and TR 2 (PINS 3, 2), are independent and specified as either:

Positive: The rising-edge option is specified for detecting a rising level transition, away from Low (Ground).
Negative: The falling-edge option is specified for detecting a falling edge level transition, toward Low (Ground).

Pulse Length Options dual independent channels specified as either:

Channel 1, Channel 2: 125 ms, 250 ms, 500 ms, 1 sec, 2.5 sec, 5 sec, 10 sec, 20 sec.

Active Pulse Options Q1 and Q2 (PINS 8, 6), are independent and specified as either:

Active High: Normally Low (Ground) and pulses High-Z (Open) for the specified pulse length.
Active Low: Normally High-Z (Open) and pulses Low (Ground) for the specified pulse length.

Truth Table

For a description of the operational states and performance of the Pulse/Timer component, see Figure 2.4.1.0-B.

Figure 2.4.1.0-B

Input	Selected Input Option	Actual Input Received	Output Response	
			Q1 or Q2 Active High-Z (Open) Normally Low (Ground) 	Q1 or Q2 Active Low (Ground) Normally High-Z (Open) 
TR 1 OR TR 2	Rising (Positive) Edge Detecting	Rising (Positive) 	Output transitions from Low (Ground) to High-Z (Open) for the specified pulse period	Output transitions from High-Z (Open) to Low (Ground) for the specified pulse period
		Falling (Negative) 	No Change: Output remains at Low (Ground)	No Change: Output remains at High-Z (Open)
	Falling (Negative) Edge Detecting	Rising (Positive)	No Change: Output remains at Low (Ground)	No Change: Output remains at High-Z (Open)
		Falling (Negative)	Output transitions from Low (Ground) to High-Z (Open) for the specified pulse period	Output transitions from High-Z (Open) to Low (Ground) for the specified pulse period
/RST 1 OR /RST 2	-	Reset = High-Z (Open)	Q1 and Q2 operate as defined above	
	-	Reset = Low (Ground)	Output is disabled (pulse cancelled) and is held at Low (Ground)	Output is disabled (pulse cancelled) and is held High-Z (Open)

2.4.1.1 Pulse/Timer, Operating Parameters

Figure 2.4.1.1-A Parametric Table	
Description	Parameters
Operating Parameters	
Operating Voltage (Max. / Nom. / Min.)	+32 VDC / +28 VDC / +18 VDC
Power Supply Input Current	4 mA (Maximum)
Reset From Power Loss at 25°C	5 sec (Minimum) at +25°C
Hold Up On Power Loss at 25°C	200 ms (Minimum)
Input Parameters	
/RST 1, /RST 2 at 25°C	55 ms (Minimum)
/TR 1, /TR 2 at 25°C	40 ms (Minimum)
* High Level Input Voltage (V_{IH}) at 25°C	+5 VDC (Minimum)
* Low Level Input Voltage (V_{IL}) at 25°C	+1.2 VDC (Maximum)
Low Level Input Current (I_{IL}) at 25°C	1mA (Maximum)
Note: All signal inputs are diode isolated	
Output Parameters	
Output Load Capacity	2.0 A (Resistive) / 1.0 A (Motor) / 0.8 A (Inductive/Lamp)
On-State Resistance at 25°C	Typical 0.07 ohms / Maximum 0.09 ohms
Off-State Resistance at 25°C	Open Drain (High-Z), Fuse-Protected MOSFET, +32 VDC Maximum
** Pulse Time Tolerance at 25°C	+/- 10%
Temperature	
Operating & Non-Operating	-55° C to +85° C
Reliability MIL-HDBK-217F, Notice 2	
Airborne Inhabited Cargo (AIC) at +40°C Continuous Operation	MTBF = 141,449 hrs
** V_{IL} and V_{IH} specifications are in reference to unit Ground.* *** Time tolerance at EMC and environmental extremes is +/- 20%.*	

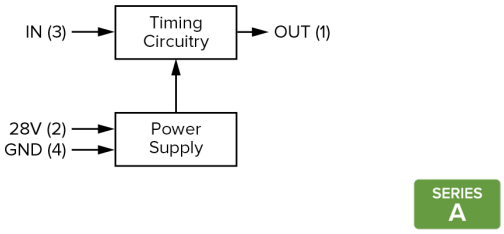
For Qualification Summary, see Appendix A

2.4.2 Time Delay

Summary Description

The NEXSYS Time Delay (TD1, TD2) is a Series A (4 Pin) device that can be specified to detect a signal level state change (trigger event) to activate the output once the unit is energized. The NEXSYS Time Delay can be specified to start the delay timer when either IN (PIN 3) detects a state change (see Figure Figure 2.4.2.0-D for signal level definitions) or upon power-up, 28V (PIN 2). OUT (PIN 1) can generate either a delayed Low (Ground) or High-Z (Open) that is initiated by a defined trigger event at IN (PIN 3). OUT (PIN 1) will remain active until the trigger condition is reversed, see Figure 2.4.2.0-A.

Figure 2.4.2.0-A



The NEXSYS Time Delay features fault-tolerant circuitry and architecture, making it ideal for applications that require stable operation, reliability, and precision. The Time Delay features an extensive range of timing options that afford design versatility; the choices range from 125 ms to 4 hrs.

The NEXSYS Time Delay (TD1, TD2) is a commercial-off-the-shelf (COTS) item. This standard catalog hardware includes features to allow for flexible interface design solutions while also meeting aircraft performance standards. The TD is designed, tested, and qualified to MIL-PRF-22885/116, MIL-PRF-22885/117, DO-160 and MIL-STD-461 requirements. Specifications are available in our MIL-PRF and DO-160 Documents page, and the qualification table is available in Appendix A.

Input Characteristics

The NEXSYS Time Delay inputs are Power (28V), Ground (GND), and Input (IN). The inputs include the following characteristics for custom timed-output control. Time Delay input circuity is diode isolated, buffered, and debounced for reliable operation. See additional sections for specific details concerning the Input/Output (I/O) interface.

28V (PIN 2): Operating Voltage (Nom.), Current Draw 4 mA (Max).
GND (PIN 4): Continuous Ground required, otherwise, inadvertent operation could occur.
IN (PIN 3): Detects trigger event, not used for Time Delay on Power-Up applications.

Output Characteristics

The NEXSYS Time Delay features a conditioned Output (OUT) that is open-drain, High-Z (Open) when not energized, and surge-protected against transients and overload conditions. The output load capacity is 0.5 A, see Figure 2.4.2.1-A (Operating Parameters) for electrical load rating types.

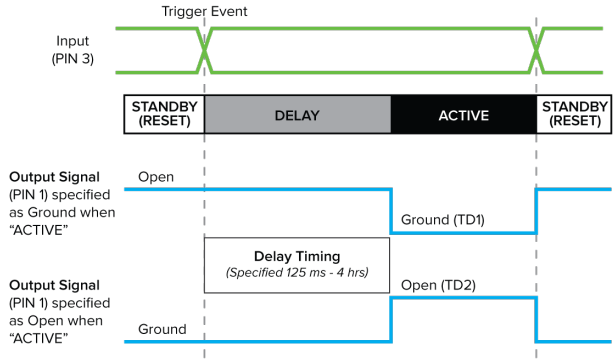
OUT (PIN 1): Specified as Active Low (Ground) or High-Z (Open) when delay timing has elapsed.

Configuration Options

The NEXSYS Time Delay features two trigger event configurations to initiate the delay timer, Time Delay on Trigger and Time Delay on Power-Up. The device also features four input level configurations, two output level configurations, and a wide range of Timing (Delay) configurations, which require constant power for operation. If power is removed or the trigger event is reversed, the timing is reset. Input and Output I/O signal level definitions are provided in the Parametric Table, see Figure 2.4.2.1-A.

Time Delay on Trigger: IN (PIN 3) detects the specified trigger event level. There are three operating states: Standby (Reset), Delay, and Active, see Figure 2.4.2.0-B.

Figure 2.4.2.0-B Time Delay on Trigger



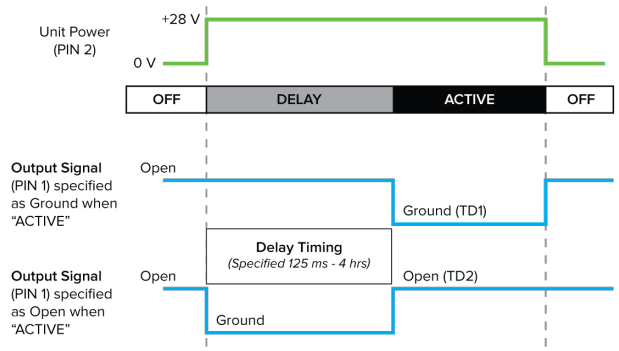
Standby (Reset): IN (PIN 3) is at the Standby (Reset) level, and OUT (PIN 1) is opposite of the specified Active level.

Delay: IN (PIN 3), the detected input level is the trigger event that initiates the timer to start. OUT (PIN 1) remains at the Delay level until the specified timing has elapsed.The delay timer will reset if the trigger event is reversed and OUT (PIN 1) will return to the Standby (Reset) level.

Active: OUT (PIN 1), specified as Low (Ground) or High-Z (Open), is Active when the specified timing has elapsed. The Active state will reset if the trigger event is reversed, and OUT (PIN 1) will return to the Standby (Reset) level.

Time Delay on Power-Up: 28V (PIN 2), operating voltage is applied, and the timer is triggered. There are two operating states: Delay and Active. IN (PIN 3) is not used for the Time Delay on Power-Up configuration, see Figure 2.4.2.0-C. The Time Delay on Power-Up option is in the Off condition when not energized.

Figure 2.4.2.0-C Time Delay on Power-Up



Note: IN (PIN 3) is not connected.

Delay: 28V (PIN 2), unit power-up is the trigger event that initiates the timer to start. OUT (PIN 1) remains at the Delay level until the specified timing has elapsed. The delay timer will reset if the trigger event is reversed, and OUT (PIN 1) will return to the Off condition.

Active: OUT (PIN 1), specified as Low (Ground) or High-Z (Open), is Active when the specified timing has elapsed. The Active state will remain until power is removed.

Off: Unit power is not applied, 28V (PIN 2) and OUT (PIN 1) is High-Z (Open).

Input Levels: IN (PIN 3) is used for the Time Delay on Trigger configuration option only, and will detect a signal level state change once the unit is energized. IN (PIN 3) features four input level configurations that transition the Standby (Reset) state to Delay/Active, see Figure 2.4.2.0-D. IN (PIN 3) detects a state-level change upon power-up. The following input level configurations do not apply to the Time Delay on Power-Up configuration.

W Configuration Code: IN (PIN 3) transitions from +28 VDC or High-Z (Open) in Standby (Reset) to Low (Ground) in Delay/Active.

P Configuration Code*: IN (PIN 3) transitions from +28 VDC in Standby (Reset) to Low (Ground) or High-Z (Open) in Delay/Active.

Figure 2.4.2.0-D Operating State, IN (PIN 3) Level

Code	STANDBY (RESET)	DELAY / ACTIVE
W	+28 VDC or High-Z (Open)	Low (Ground)
P	+28 VDC Must be same power source as PIN 2	Low (Ground) or High-Z (Open)
D	Low (Ground) or High-Z (Open)	+28 VDC Must be same power source as PIN 2
G	Low (Ground)	+28 VDC or High-Z (Open)

D Configuration Code*: IN (PIN 3) transitions from Low (Ground) or High-Z (Open) in Standby (Reset) to +28 VDC in Delay/Active.

G Configuration Code: IN (PIN 3) transitions from Low (Ground) in Standby (Reset) to +28 VDC or High-Z (Open) in Delay/Active.

**Must be the same +28 VDC source as PIN 2 (28V).*

Output Levels: OUT (PIN 1) features two output level configurations that transition Standby (Reset) or Delay to the Active state, see Figure 2.4.2.0-E.

TD1: OUT (PIN 1), Low (Ground) when Active, and High-Z (Open) when in Standby or Delay.

TD2: OUT (PIN 1), High-Z (Open) when Active, and Low (Ground) when in Standby or Delay.

Figure 2.4.2.0-E Operating State, OUT (PIN 1)

Code	STANDBY (RESET) or DELAY	ACTIVE
TD1	High-Z (Open)	Low (Ground)
TD2	Low (Ground)	High-Z (Open)

Timing (Delay): Delay timing configurations range from 125 ms to 4 hrs and are available in four delay timing increments.

Milliseconds: 125*, 250*, 500
Seconds: 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 15, 20, 30
Minutes: 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 15, 20, 30
Hours: 1, 2, 4

**Not available in the Time Delay on Power-up configuration.*

2.4.2.1 Time Delay, Operating Parameters

Figure 2.4.2.1-A	
Description	Parameters
Operating Parameters	
Operating Voltage (Max./Nom./ Min.)	+32 VDC /+28 VDC/+18 VDC
Power Supply Input Current	4 mA (Maximum)
Reset From Power Loss at 25°C	5 sec (Minimum) at +25°C
Hold Up On Power Loss at 25°C	200 ms (Minimum)
Input Parameters	
Input Timing at 25°C	10 ms (Maximum)
* High Level Input Voltage (V_{IH}) at 25°C	1 mA (Maximum)
* Low Level Input Voltage (V_{IL}) at 25°C	< +1.5 VDC
Low Level Input Current (I_{IL}) at 25°C	> +8 VDC
All Pulled-up inputs are diode isolated	
Output Parameters	
Output Load Capacity	IntelliFET® 0.5 A (Resistive/Motor/Inductive/Lamp)
On-State Resistance at 25°C	Typical 0.4 ohms / Maximum 0.6 ohms
Off-State Resistance at 25°C	Open Drain (High-Z), Self-Protected IntelliFET®, +32 VDC Maximum
** Delay Time Tolerance at 25°C	+/- 5%
Temperature	
Operating	-55°C to +85°C
Non-operating	-55°C to +125°C
Reliability MIL-HDBK-217F, Notice 2	
Airborne Inhabited Cargo (AIC) at +40°C Continuous Operation	MTBF = 321,986 hrs

** V_{IL} and V_{IH} specifications are in reference to unit Ground.*

*** Delay time tolerance at EMC and environmental extremes is +/- 10%.*

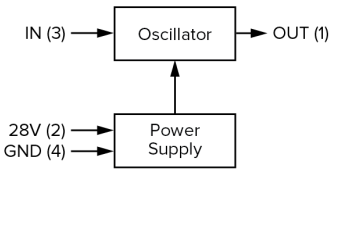
For Qualification Summary, see Appendix A

2.4.3 Square Wave Oscillator

Summary Description

The NEXSYS Square Wave Oscillator (CT1, CT2) is a Series A (4 Pin) device that can be specified to detect a signal level state change (trigger event) to activate the output once the unit is energized. OUT (PIN 1) can be specified to begin oscillating when IN (PIN 3) detects a state change, see Figure 2.4.3.0-C for signal level definitions. OUT (PIN 1) can generate an oscillating High-Z (Open) to Low (Ground) or Low (Ground) to High-Z (Open) at a specified frequency initiated by a defined trigger event at IN (PIN 3). OUT (PIN 1) will remain active until the trigger condition is reversed, see Figure 2.4.3.0-A.

Figure 2.4.3.0-A



The NEXSYS Square Wave Oscillator features fault-tolerant circuitry and architecture, making it ideal for applications that require stable operation, reliability, and precision. The Square Wave Oscillator offers a range of frequency/cycle options from 0.25 Hz to 500 Hz.

The NEXSYS Square Wave Oscillator (CT1, CT2) is a commercial-off-the-shelf (COTS) item. This standard catalog hardware includes features to allow for flexible interface design solutions while also meeting aircraft performance standards. The CT is designed, tested, and qualified to MIL-PRF-22885/116, MIL-PRF-22885/117, DO-160 and MIL-STD-461 requirements. Specifications are available in our MIL-PRF and DO-160 Documents page, and the qualification table is available in Appendix A.

Input Characteristics

The NEXSYS Square Wave Oscillator inputs are Power (28V), Ground (GND), and Input (IN). The inputs include the following characteristics for custom oscillating-output control. Square Wave Oscillator input circuity is diode isolated, buffered, and debounced for reliable operation. See additional sections for specific details concerning the Input/Output (I/O) interface.

28V (PIN 2): Operating Voltage (Nom.), Current Draw 4 mA (Max).
GND (PIN 4): Continuous Ground required, otherwise, inadvertent operation could occur.
SENSE (PIN 3): Detects trigger event.

Output Characteristics

The NEXSYS Square Wave Oscillator features a conditioned Output (OUT) that is open-drain High-Z (Open) when not active and surge-protected against transients and overload conditions. When Active, OUT Oscillates between Ground and Open. The output load capacity is 0.5 A, see Figure 2.4.3.1-A (Operating Parameters) for electrical load rating types.

OUT (PIN 1): Oscillates Low (Ground)/High-Z (Open) when triggered.

Configuration Options

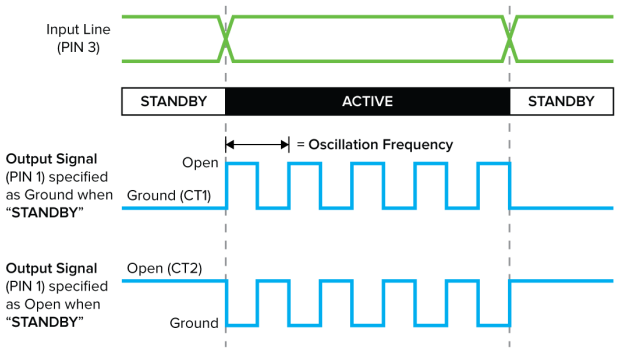
The NEXSYS Square Wave Oscillator features two trigger event configurations to initiate oscillation, Oscillate on Trigger and Oscillate on Power-Up. The device also features four input level configurations, two output level configurations, and a wide range of oscillation configurations, which require constant power for operation. Input and output I/O signal level definitions are provided in the Parametric Table, see Figure 2.4.3.1-A.

Oscillate on Trigger: IN (PIN 3) detects the specified trigger event level. There are two operating states: Standby and Active, see Figure 2.4.3.0-B.

Standby: IN (PIN 3) is at the Standby level, and OUT (PIN 1) is specified as either steady-state Low (Ground) or High-Z (Open).

Active: OUT (PIN 1) oscillates between Low (Ground) and High-Z (Open) at the specified oscillation frequency. Oscillation will terminate if the trigger event is reversed, and OUT (PIN 1) will return to the Standby level.

Figure 2.4.3.0-B



Input Levels: IN (PIN 3) features four input level configurations that transition Standby state to Active, see Figure 2.4.3.0-C. IN (PIN 3) detects a state-level change upon power-up.

W Configuration Code: IN (PIN 3) transitions from +28 VDC or High-Z (Open) in Standby to Low (Ground) in Active.

P Configuration Code*: IN (PIN 3) transitions from +28 VDC in Standby to Low (Ground) or High-Z (Open) in Active.

D Configuration Code*: IN (PIN 3) transitions from Low (Ground) or High-Z (Open) in Standby to +28 VDC in Active.

Figure 2.4.3.0-C Operating State, IN (PIN 3) Level

Code	Oscillation STANDBY	Oscillation ACTIVE
W	+28 VDC or High-Z (Open)	Low (Ground)
P	+28 VDC Must be same power source as PIN 2	Low (Ground) or High-Z (Open)
D	Low (Ground) or High-Z (Open)	+28 VDC Must be same power source as PIN 2
G	Low (Ground)	+28 VDC or High-Z (Open)

G Configuration Code: IN (PIN 3) transitions from Low (Ground) in Standby to +28 VDC or High-Z (Open) in Active.

**Must be the same +28 VDC source as +28 VDC (PIN 2).*

Output Levels: OUT (PIN 1) features two output level configurations that transition Standby to the Active state.

CT1: OUT (PIN 1) is Low (Ground) in Standby and Oscillates Low (Ground)/High-Z (Open) when Active.

CT2: OUT (PIN 1), High-Z (Open) in Standby, and Oscillates Low (Ground)/High-Z (Open) when Active.

Figure 2.4.3.0-D Operating State, OUT (PIN 1)

Code	Oscillation STANDBY	Oscillation ACTIVE
CT1	Low (Ground)	Oscillating, Low (Ground) to High-Z (Open)
CT2	High-Z (Open)	Oscillating, Low (Ground) to High-Z (Open)

Oscillation Frequency: Oscillation configurations range from 0.25 Hz to 500 Hz and are available in eight increments, see Figure 2.4.3.0-E.

Figure 2.4.3.0-E	
Frequency (Cycles / Sec)	Period (Sec / Cycle)
0.25 Hz	4
0.5 Hz	2
1 Hz	1
2 Hz	0.5
4 Hz	0.25
10 Hz	0.1
100 Hz	0.01
500 Hz	0.002

2.4.3.1 Square Wave Oscillator, Operating Parameters

Figure 2.4.3.1-A	
Description	Parameters
Operating Parameters	
Operating Voltage (Max./Nom./ Min.)	+32 VDC /+28 VDC/+18 VDC
Power Supply Input Current	4 mA (Maximum)
Reset From Power Loss at 25°C	5 sec (Minimum) at +25°C
Hold Up On Power Loss at 25°C	200 ms (Minimum)
Input Parameters	
Input Timing at 25°C	10 ms (Maximum)
* High Level Input Voltage (V_{IH}) at 25°C	1 mA (Maximum)
* Low Level Input Voltage (V_{IL}) at 25°C	< +1.5 VDC
Low Level Input Current (I_{IL}) at 25°C	> +8 VDC
All Pulled-up inputs are diode isolated	
Output Parameters	
Output Load Capacity	IntelliFET® 0.5 A (Resistive/Motor/Inductive/Lamp)
On-State Resistance at 25°C	Typical 0.4 ohms / Maximum 0.6 ohms
Off-State Resistance at 25°C	Open Drain (High-Z), Self-Protected IntelliFET®, +32 VDC Maximum
Cycle Time Tolerance at 25°C	+/- 5%
Temperature	
Operating	-55°C to +85°C
Non-operating	-55°C to +125°C
Reliability MIL-HDBK-217F, Notice 2	
Airborne Inhabited Cargo (AIC) at +40°C Continuous Operation	MTBF = 321,986 hrs
** V_{IL} and V_{IH} specifications are in reference to unit Ground.*	

For Qualification Summary see Appendix A

2.5 Sensing Components

Components that sense Direct Current (DC) voltage and current levels to trigger a discrete output when the detected level is above or below a specified setpoint.

Sensing components include:

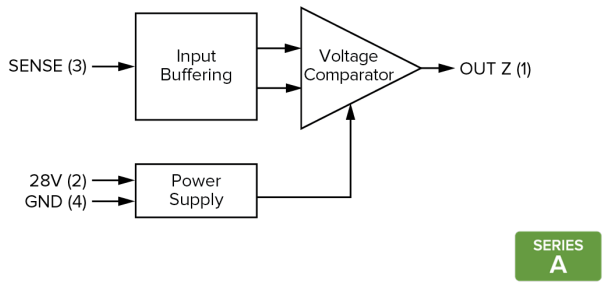
- Voltage Sensor
- Current Sensor

2.5.1 Voltage Sensor

Summary Description

The NEXSYS Voltage Sensor (VSD1, VSD2) is a Series A (4 Pin) solid-state, low-side direct current (DC) voltage sensor, developed to enhance avionics design flexibility by offering undervoltage and overvoltage detection. The Voltage Sensor compares DC voltage in a linear relationship between the specified setpoint and the voltage that is being monitored by the SENSE input. The fast-response output provides a discrete signal that transitions from High-Z (Open) to Low (Ground) when the input detects voltage that is above or below the specified setpoint, see Figure 2.5.1.0-A.

Figure 2.5.1.0-A



The NEXSYS Voltage Sensor features fault-tolerant circuitry and architecture that provides low-drift voltage sensing over temperature. The Voltage Sensor also offers a range of setpoint options from +50 mVDC to +48 VDC.

The NEXSYS Voltage Sensor (VSD1, VSD2) is a commercial-off-the-shelf (COTS) item. This standard catalog hardware includes features to allow for flexible interface design solutions while also meeting aircraft performance standards. The VSD is designed, tested, and qualified to MIL-PRF-22885/116, MIL-PRF-22885/117, DO-160 and MIL-STD-461 requirements. Specifications are available in our MIL-PRF and DO-160 Documents page, and the qualification table is available in Appendix A.

There are two configuration types:

- VSD1 performs overvoltage and undervoltage detection from +1 to 48 VDC.
- VSD2 performs overvoltage and undervoltage detection from +50 mVDC to 1000 mVDC (1 VDC).

Input Characteristics

The NEXSYS Voltage Sensor inputs are Power (28V), Ground (GND) and Sense (SENSE). The inputs include the following characteristics for custom voltage sensing and output control. Voltage Sensor input circuity is diode isolated, buffered, and debounced for reliable operation. See additional sections for specific details concerning the Input/Output (I/O) interface.

28V (PIN 2): Operating Voltage (Nom.), VSD1 = Current Draw 2 mA (Max) and VSD2 = Current Draw 4 mA (Max).
GND (PIN 4): Continuous Ground required, otherwise, inadvertent operation could occur.
SENSE (PIN 3): Detects DC input voltage and includes a hysteresis band to prevent signal chatter.

Output Characteristics

The NEXSYS Voltage Sensor features a conditioned Output Z (OUT Z) that is open-drain High-Z (Open) when not active, and surge-protected against transients and overload conditions. The output load capacity is 2.0 A for VSD1 and 0.5 A for VSD2, see Figure 2.5.1.1-A (Operating Parameters) for electrical load rating types.

OUT Z (PIN 1): Active = Low (Ground), Not Active = High-Z (Open)

Configuration Options

The NEXSYS Voltage Sensor features an extensive range of setpoints to provide an Active Low (Ground) output when the specified undervoltage or overvoltage condition is detected, as detailed below. The Voltage Sensor can also be configured to perform wide hysteresis and current sensing.

Overvoltage: OUT Z (PIN 1) = Low (Ground), when the voltage monitored by SENSE (PIN 3) is ABOVE the specified setpoint, see Figure 2.5.1.0-B.

Undervoltage: OUT Z (PIN 1) = Low (Ground), when the voltage monitored by SENSE (PIN 3) is BELOW the specified setpoint, seeFigure 2.5.1.0-C.

Wide Hysteresis: When combined with a NEXSYS Electronic Latch, the Voltage Sensor can perform wide hysteresis with different pull-in and drop-out levels for enhanced system noise tolerance.

Current Sensing[1,2]**:** When combined with an external shunt resistor (not included), the NEXSYS Voltage Sensor (VSD2) can perform as a current sensor by wiring an external resistor to a VSD2, see Figure 2.5.1.0-D. The VSD2 will measure the voltage drop across the external resistor as compared to the Ground supplied to the device. Common industry shunt resistors and standard VSD2 configurations are listed below as an example of how a current sense solution can be achieved, see Figure 2.5.1.0-E.

Figure 2.5.1.0-B

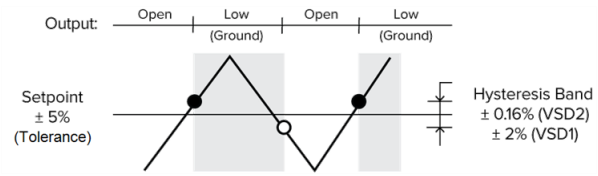


Figure 2.5.1.0-C

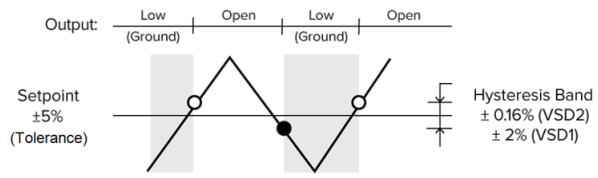


Figure 2.5.1.0-D

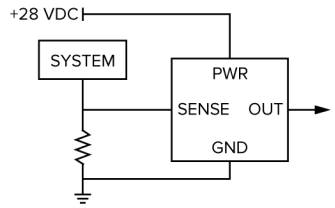


Figure 2.5.1.0-E

Current Sense Target	Customer Shunt Resistor	Example NEXSYS VSD2 Configuration
10 A	0.01 ohms (> 1 W)	VSD2/0100/A (100 mV)
20 A	0.01 ohms (> 4 W)	VSD2/0200/A (200 mV)
30 A	0.01 ohms (> 9 W)	VSD2/0300/A (300 mV)
40 A	0.01 ohms (> 16 W)	VSD2/0400/A (400 mV)

Voltage Setpoints[3]**:** two configurations (VSD1, VSD2) that offer an extensive range of voltage setpoints in increments between +50 mVDC to +48 VDC.

VSD1, performs overvoltage and undervoltage detection from +1 to 48 VDC, at the specified setpoint increments:

+0.5 VDC increments: +1.0, 1.5, 2.0, 2.5, 3.0, 3.5, 4.0, 4.5. 5.0, 5.5, 6.0, 6.5, 7.0, 7.5, 8.0, 8.5, 9.0, 9.5 VDC.
+1.0 VDC increments: +10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30 VDC.
+2.0 VDC increments: +32, 34, 36, 38, 40 VDC.
+4.0 VDC increments: +44, 48 VDC.

VSD2, performs overvoltage and undervoltage detection from +50 mVDC to 1000 mVDC (1 VDC), at the specified setpoint increments:

+10 mVDC increments: +50, 60, 70, 80, 90 mVDC.
+50 mVDC increments: +100, 150, 200, 250, 300, 350, 400, 450, 500, 550, 600, 650, 700, 750, 800, 850, 900, 950, 1000 mVDC.

1. The NEXSYS Current Sensor (CS1) features an integrated resistor (vs. external shunt) for undercurrent and overcurrent sensing, with setpoint options ranging from 10mA to 1000mA (1A), see Current Sensor.
2. Because the VSD2 SENSE Input and GND share the same Ground lead, current flowing through the Ground lead should be limited to 10mA to minimize measurement error. Ground of VSD2 and sensed device must be the same to achieve maximum accuracy.
3. The VSD1 Nominal Rising Voltage setpoint tolerance of SENSE (PIN 3) is +/- 5%. Falling Voltage Hysteresis -3% Max (-2% Typical), measured from the setpoint after the inclusion of the Rising Voltage setpoint. The VSD2 setpoint tolerance of SENSE (PIN 3) is +/- 5%. The VSD2 has a hysteresis band (+/- 0.16%) that will prevent a state change until the sensed voltage exceeds hysteresis. Tolerance at EMC and Environmental extremes is +/- 10%.

2.5.1.1 Voltage Sensor, Operating Parameters

Figure 2.5.1.1-A	
Description	Parameters
Operating Parameters	
Operating Voltage (Max./Nom./ Min.)	+32 VDC /+28 VDC/+18 VDC
Power Supply Input Current	**VSD1:** 2 mA (Maximum) **VSD2:** 4 mA (Maximum)
Reset From Power Loss at 25°C	5 sec (Minimum) at +25° C
Hold Up On Power Loss at 25°C	**VSD1:** 200 ms (Minimum) **VSD2:** 50 ms (Minimum)
Input Parameters	
Sense Voltage	**VSD1:** +1 to 48 VDC **VSD2:** +50 to 1000 mVDC
Rising Voltage Setpoint Tolerance (VSD1)	+/- 5%
Falling Voltage Hysteresis (VSD1) *Note: Measured from the Setpoint after inclusion of the Rising Voltage Setpoint Tolerance above.*	-3% (Maximum) (-2% Typical)
Setpoint Tolerance (VSD2)	+/- 5%
Hysteresis Band (VSD2)	+/- 0.16%
Typical Input Impedance (T_{SENSE}, Voltage Drop)	**VSD1:** 200 kiloohms **VSD2:** 100 kiloohms to Ground
Transition Time Sense to Out (T_{SENSE})	**VSD1:** 5 ms (Maximum) **VSD2:** 10 ms (Maximum)
All Pulled-up inputs are diode isolated	
Output Parameters	
Output Load Capacity	**VSD1:** Fused MOSFET 2.0 A (Resistive), 0.8 A (Inductive) **VSD2:** IntelliFET® 0.5 A (Resistive / Motor / Inductive / Lamp)
On-State Resistance at 25°C	**VSD1:** Typical 0.07 ohms / Maximum 0.09 ohms **VSD2:** Typical 0.4 ohms / Maximum 0.6 ohms
Off-State Resistance at 25°C	**VSD1:** Open Drain (High-Z), Fuse-Protected MOSFET, +32 VDC Maximum **VSD2:** Open Drain (High-Z), Self-Protected IntelliFET®, +32 VDC Maximum
Temperature	
Operating	-55° C to +85° C
Non-operating	-55° C to +85° C
Reliability MIL-HDBK-217F, Notice 2	
Airborne Inhabited Cargo (AIC) at +40°C Continuous Operation	**VSD1:** MTBF = 432,460 hrs **VSD2:** MTBF = 422,347 hrs

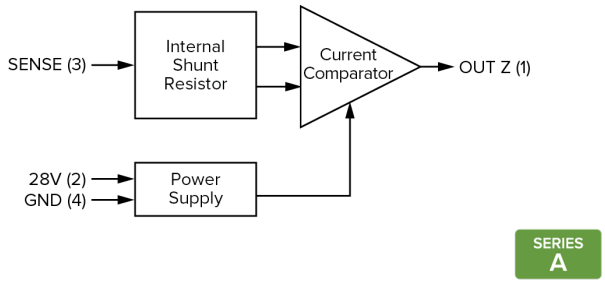
For Qualification Summary, see Appendix A

2.5.2 Current Sensor

Summary Description

The NEXSYS Current Sensor (CS1) is a Series A (4 Pin) solid-state, low-side direct current (DC) sensor developed to enhance avionics design flexibility by offering undercurrent and overcurrent detection. The CS1 compares electric current in a linear relationship between the specified setpoint and the current that is being monitored by the SENSE input. The fast-response output provides a discrete signal that transitions from Open to Ground when the input detects current that is above or below the specified setpoint, see Figure 2.5.2.0-A.

Figure 2.5.2.0-A



The NEXSYS Current Sensor features fault-tolerant circuitry and architecture that provides low-drift current sensing over temperature. The CS1 also offers an extensive range of setpoint options that afford design versatility; the choices range from 10 mA to 1000 mA (1.0 A).

The NEXSYS Current Sensor (CS1) is a commercial-off-the-shelf (COTS) item. This standard catalog hardware includes features to allow for flexible interface design solutions while also meeting aircraft performance standards. The CS is designed, tested, and qualified to MIL-PRF-22885/116, MIL-PRF-22885/117, DO-160 and MIL-STD-461 requirements. Specifications are available in our MIL-PRF and DO-160 Documents page, and the qualification table is available in Appendix A.

Input Characteristics

The NEXSYS Current Sensor inputs are Power (28V), Ground (GND) and Sense (SENSE). The inputs include the following characteristics for custom current sensing and output control. Current Sensor input circuity is diode isolated, buffered, and debounced for reliable operation. See additional sections for specific details concerning the Input/Output (I/O) interface.

28V (PIN 2): Operating Voltage (Nom.), Current Draw 2 mA (Max).
GND (PIN 4): Continuous Ground required, otherwise, inadvertent operation could occur.
SENSE (PIN 3): Detects DC input current and includes a hysteresis band to prevent signal chatter.

Output Characteristics

The NEXSYS Current Sensor features a conditioned Output Z (OUT Z) output that is open-drain High-Z (Open) when not active, and surge-protected against transients and overload conditions. The output load capacity is 0.5 A, see Figure 2.5.2.1-A (Operating Parameters) for electrical load rating types.

OUT Z (PIN 1): Active = Low (Ground), Not Active = High-Z (Open)

Configuration Options

The NEXSYS Current Sensor features an extensive range of setpoints to provide an Active Low (Ground) output when the specified undercurrent or overcurrent condition is detected, as detailed below. The Current Sensor can also be configured to perform wide hysteresis.

Overcurrent: Overcurrent: OUT Z (PIN 1) = Low (Ground), when current monitored by SENSE (PIN 3) is ABOVE the specified setpoint, see Figure 2.5.2.0-B.

Undercurrent: OUT Z (PIN 1) = Low (Ground), when current monitored by SENSE (PIN 3) is BELOW the specified setpoint, see Figure 2.5.2.0-C.

Wide Hysteresis: When combined with a NEXSYS Electronic Latch, the Current Sensor can perform wide hysteresis with different pull-in and drop-out levels for enhanced system noise tolerance.

Current Setpoints[1]: Two increment options that offer an extensive range of current setpoints in increments of 10 mA between 10 to 90 mA and in increments of 50 mA between 100 to 1000 mA.

10 mA Setpoints: 10, 20, 30, 40, 50, 60, 70, 80 and 90 mA.
50 mA Setpoints: 100, 150, 200, 250, 300, 350, 400, 450, 500, 550, 600, 650, 700, 750, 800, 850, 900, 950, 1000 mA.

Figure 2.5.2.0-B

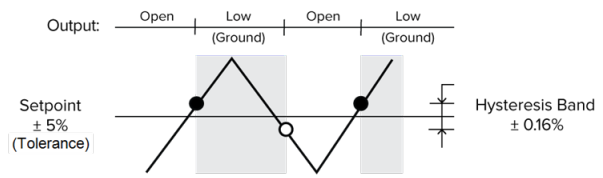
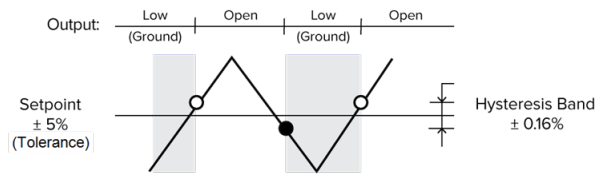


Figure 2.5.2.0-C



1. The setpoint tolerance of SENSE (PIN 3) is +/- 5%. The unit has a hysteresis band (+/- 0.16%) that will prevent a state change until the sensed current exceeds hysteresis. Tolerance at EMC and Environmental extremes is +/- 10%.

2.5.2.1 Current Sensor, Operating Parameters

Figure 2.5.2.1-A	
Operating Parameters	
Operating Voltage (Max./Nom./ Min.)	+32 VDC /+28 VDC/+18 VDC
Power Supply Input Current	4 mA (Maximum)
Reset From Power Loss at 25°C	5 sec (Minimum) at +25°C
Hold Up On Power Loss at 25°C	50 ms (Minimum)
Input Parameters	
Sense Current	10 mA to 1000 mA (1.0 A)
Setpoint Tolerance	+/- 5%
Hysteresis Band	+/- 0.16%
Typical T_{SENSE}, Voltage Drop	50 mV to Ground
Transition Time Sense to Out (T_{SENSE})	10 ms (Maximum)
All Pulled-up inputs are diode isolated	
Output Parameters	
Output Load Capacity	IntelliFET® 0.5 A (Resistive/Motor/Inductive/Lamp)
On-State Resistance at 25°C	Typical 0.4 ohms / Maximum 0.6 ohms
Off-State Resistance at 25°C	Open Drain (High-Z), Self-Protected IntelliFET®, +32 VDC Maximum
Temperature	
Operating	-55°C to +85°C
Non-operating	-55°C to +125°C
Reliability MIL-HDBK-217F, Notice 2	
Airborne Inhabited Cargo (AIC) at +40°C Continuous Operation	MTBF = 422,347 hrs

For Qualification Summary, see Appendix A

2.6 Passive Components

Passive components integrated into a form factor design that is optimized for packaging inside NEXSYS and VIVISUN housings.

Passive components include:

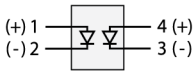
- Diode Pack
- Terminal Block

2.6.1 Diode Pack

Summary Description

The NEXSYS Diode Pack (DP2C, DP2M) is a Series A (4 Pin) component designed to replace external in-line harness diodes and enhance avionics design flexibility. Each Diode Pack component contains two independent diode circuits, see Figure 2.6.1.0-A.

Figure 2.6.1.0-A



SERIES A

The NEXSYS Diode Pack (DP2C, DP2M) is commercial-off-the-shelf (COTS) item. This standard catalog hardware includes features to allow for flexible interface design solutions while also meeting aircraft performance standards. The DP is designed, tested, and qualified to MIL-PRF-22885/116, MIL-PRF-22885/117, DO-160 and MIL-STD-461 requirements. Specifications are available in our MIL-PRF and DO-160 Documents page, and the qualification table is available in Appendix A.

Input/Output (I/O) Characteristics

NEXSYS Diode Packs are manufactured with the polarity arranged from Anode (PIN 1, 4) to Cathode (PIN 2, 3), see Figure 2.6.1.1-A.

Configuration Options

The NEXSYS Diode Pack is available in two different configurations, commercial and military.

Commercial Diodes (DP2C)
Two 1N6484 glass passivized diodes (Vishay® or equivalent). Consult manufacturer's datasheet for detailed diode specifications. 1.0 A average forward current

Military Diodes (DP2M)
Two JANTX1N5621 Hermetic glass sealed diodes (Microsemi or equivalent). Consult manufacturer's datasheet for detailed diode specifications. The integrated JEDEC Registered diodes feature triple-layer passivation and inherently radiation hard.

2.6.1.1 Diode Pack, Operating Parameters

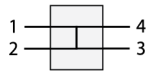
Figure 2.6.1.1-A		
Description	Parameters	
Operating Parameters		
Insulation Resistance	5,000 megaohms at +25° C	
Dielectric Withstanding	1,000 V_{RMS}	
Operating & Non Op. Temp.	-55° C to +85° C	
Electrical Parameters		
	Comm'l. (1N6484)*	Military (JANTX1N5621)*
Current Rating (Maximum)	1.0 A	1.0 A
Working Voltage	+1,000 VDC	+800 VDC
Breakdown Voltage	+1,000 VDC	+880 VDC Peak
Electrical and Environmental Performance		
Meets or exceeds defines levels for RTCA/D0-160 and MIL-STD-202		
**Consult manufacturer's data sheet for detailed diode specifications.*		

2.6.2 Terminal Block

Summary Description

The NEXSYS Terminal Block (TB4) is a Series A (4 Pin) component designed to eliminate the need for external splice and terminal junction components. The Terminal Block is rated for a maximum of 5 A and provides the ability to bus a single input to three outputs, see Figure 2.6.2.0-A. Twenty-two pin NEXSYS Multinode Terminal Block Modules are also available for higher density termination applications, see Figure 2.6.2.0-B.

Figure 2.6.2.0-A



SERIES A

The NEXSYS Terminal Block (TB4, MPTB) is commercial-off-the-shelf item. This standard catalog hardware includes features to allow for flexible interface design solutions while also meeting aircraft performance standards. The TB is designed, tested, and qualified to MIL-PRF-22885/116, MIL-PRF-22885/117, DO-160 and MIL-STD-461 requirements. Specifications are available in our MIL-PRF and DO-160 Documents page, and the qualification table is available in Appendix A.

Input/Output (I/O) Characteristics

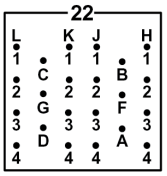
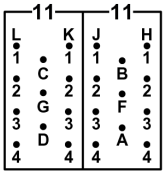
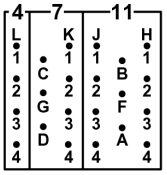
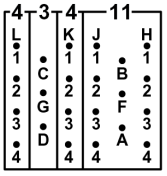
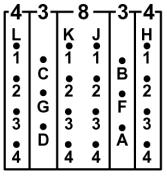
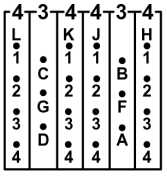
NEXSYS Terminal Blocks are manufactured with four terminals (1-4) tied together, see Figure 2.6.2.0-A. NEXSYS Multinode Terminal Block Modules are manufactured with up to twenty-two (22) terminals tied together in one (1) to six (6) node segments, see Figure 2.6.2.0-B.

Configuration Options

The NEXSYS Terminal Block is available in the 4-splice configuration. NEXSYS Multinode Terminal Block Modules are available in 3-splice to 22-splice configurations. External terminal block configurations are also available.

Terminal Block 4 (TB4)
Four (4) termination splice, rated at 5.0 A (Max) and 1.0 (Max) when used with SR429 Signal Converters.

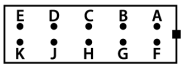
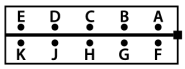
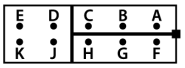
Multinode Terminal Block Modules (22 Pin)
Twenty-two pin Terminal Block Modules are available in one (1) to six (6) node segments and rated at 7.5 A (Max), see Figure 2.6.2.0-B. Multinode Terminal Block Modules can be specified with the Connector Plug (P/N: 18-440) included or separately for advance wire harness manufacture without the necessity of having the Module housing. The solderless termination interface uses MIL-C-39029/22-192 (AAI P/N: 18-219) sockets crimped onto 20, 22, or 24 gauge wire. Additional details concerning Connector Plug Termination and Installation are available, see Section 4.2 and 4.3. Each Module is provided with an in-line boot (P/N: 22-004). The Modules are also compatible with M81714 Tracks (Type 1), and additional NEXSYS Module Installation and Mounting Options, see Section 3.3.

Figure 2.6.2.0-B		
Configuration	**Military P/N**	**AAI P/N**
 ONE (1) NODE SEGMENT	M22885-XXXX/116(1)	LM-1210-E-MPTB1(2)
 TWO (2) NODE SEGMENTS	M22885-XXXX/116(1)	LM-1210-E-MPTB2(2)
 THREE (3) NODE SEGMENTS	M22885-XXXX/116(1)	LM-1210-E-MPTB3(2)
 FOUR (4) NODE SEGMENTS	M22885-XXXX/116(1)	LM-1210-E-MPTB4(2)
 FIVE (5) NODE SEGMENTS	M22885-XXXX/116(1)	LM-1210-E-MPTB5(2)
 SIX (6) NODE SEGMENTS	M22885-XXXX/116(1)	LM-1210-E-MPTB6(2)
Crimp Sockets	M39029/22-192	18-219(3)
(1) Terminal Blocks are designed and tested to the referenced military specifications and are compatible with M81714 Tracks (Type 1).		
(2) Terminal Blocks can be specified with the Connector Plug (P/N: 18-440) included, as referenced in the table or separately. Replace the "E" with an "X" (i.e., LM-1210-X-MPTB1) in the part number to specify the Connector Plug separately.		
(3) Connector Plugs (P/N: 18-440) are supplied with sealing plugs, but *NOT* crimp sockets. Crimp sockets are ordered using P/N: 18-219.		

Terminal Junction Modules

Three versions of 7.5 A, 10-pin, rail-mounted terminal blocks. Crimp socket size differs from NEXSYS components; consult MIL-T-81714 and MIL-T-81714/2 for detailed product specifications, see Figure 2.6.2.0-C.

Figure 2.6.2.0-C

Configuration	Military P/N	AAI P/N
	M81714/2-DA1(3)	22-017(1)
	M81714/2-DB1(3)	22-018(1)
	M81714/2-DC1(3)	22-019(1)
Crimp Sockets(2)	M39029/1-101	22-120

(1) Terminals Blocks are supplied with crimp sockets and sealing plugs. Additional crimp sockets for dedicated terminal blocks are ordered using Applied Avionics P/N: 22-120.

(2) These crimp sockets are compatible with the dedicated external terminal blocks listed. All VIVISUN Body and NEXSYS Module components, including the 4-pin integrated terminal block (TB4), use MIL-C-39029/22-192 (Applied Avionics P/N: 18-219) crimp sockets, ordered separately.

(3) Consult MIL-T-81714 and MIL-T-81714/2 for detailed product specifications; temperature range -65°C to +200°C, insulation resistance 5,000 megaohms at +25°C, and dielectric withstanding 1,500 V_{RMS}.

2.6.2.1 Terminal Block, Operating Parameters

Figure 2.6.2.1-A	
Description	Parameters
Operating Parameters	
Insulation Resistance	5000 megaohms at 25° C
Dielectric Withstanding	1000 V_{RMS}
Operating & Non Op. Temp.	-55° C to +85° C
Electrical Parameters	
Terminal Block 4 (TB4) Current Rating (Max)	5.0 A (Maximum) and 1.0 (Maximum) with SR429 Signal Converters
Multinode TB Module Current Rating (Max)	7.5 A (Maximum) /Node
Electrical and Environmental Performance	
Meets or exceeds defined levels for RTCA/D0-160 and MIL-STD-202	

3.0 NEXSYS® Module and Configurations

Summary Description

The NEXSYS Module is a thermoplastic enclosure designed to host a single or multiple NEXSYS components.

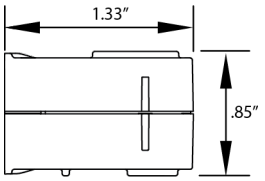
NEXSYS Modules can be configured with any of the mix-and-match NEXSYS components.

NEXSYS Modules can be wired to other NEXSYS Modules or VIVISUN switches and indicators, to design solutions with additional system functionality.

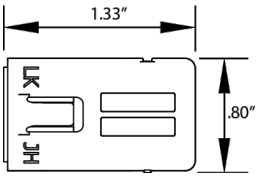
NEXSYS Modules can be mounted three different ways. Every module comes with a boot for in-harness wiring.

Dimensions

Figure 3.0.0.0-A



Side View



Top View

Operating Parameters

The following table describes the physical, environmental and performance characteristics of the NEXSYS Module.

Figure 3.0.0.0-B

Description	Parameters
Physical	
Weight (Includes Connector Plug)	Module: 14 grams (0.5 ounces Maximum) Module and boot: 22 grams (0.8 ounces Maximum) Module and bracket: 22 grams (0.8 ounces Maximum)
Materials	Module Housing: Thermoplastic Module Boot: UL V-0 Rated Vinyl Module Bracket: Stainless Steel
Environmental	
Temperature	Operating/Non-operating -55C to +85C
Altitude	-15,000 to +55,000 ft
Salt and Humidity	Humidity: 240 hrs, Salt: 96 hrs
Shock	20 G Sawtooth, 75 G half-sine
Vibration	10 to 2000 Hz 15 G
Electrical and Functional Performance	
Functional descriptions and test levels are defined in the applicable component sections of this Technical Guide. Testing meets or exceeds the defined levels for RTCA/DO-160, MIL-STD-202 and MIL-STD-810.	

3.1 Component Configurations

NEXSYS Modules can accommodate 10 specific component combinations based on the Series of components specified as shown below. Modules have four positions (H, J, K and L), each with four pins. If a position is unused, no pins will be placed in those positions, therefore a module can have 4, 8, 12 or 16 pins. Series N and Series R components must be specified alone in a NEXSYS Module due to larger dimensions.

Figure 3.1.0.0-A

	H J K L
Series A only components	SERIES A OPEN OPEN OPEN - or - SERIES A SERIES A OPEN OPEN - or - SERIES A SERIES A SERIES A OPEN - or - SERIES A SERIES A SERIES A SERIES A
Series C components	OPEN SERIES C OPEN - or - SERIES A SERIES C OPEN - or - SERIES A SERIES C SERIES A - or - SERIES C SERIES C
Series N components	SERIES N
Series R components	SERIES R

3.2 Termination

NEXSYS Modules require a specially keyed solderless Connector Plug (P/N 18-440). Plugs can be ordered with NEXSYS Modules or ordered separately. An Extraction Tool (P/N 18-234) is required to remove the Connector Plug from the NEXSYS Module. The Connector Plug can be inserted into the NEXSYS module before or after insertion into any of the mounting options.

Figure 3.2.0.0-A

Pins	NEXSYS Module	Connector Plug
A-G	Not Used	 P/N 18-440
H1-H4, L1-L4, J1-J4, K1-K4	NEXSYS Component Contacts MIL-C-39029/22-192 (P/N 18-219)	

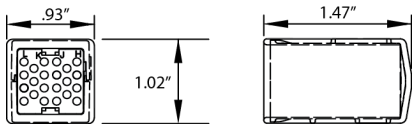
Connector Plug designed to accept 20, 22, or 24 gauge wire terminated with MIL-C-39029/22-192 (P/N 18-219) crimp sockets. Wires with the sockets crimped on can be inserted into and extracted from the Connector Plug using a M81969/14-02 (P/N 18-216) extraction tool.

3.3 Installation and Mounting Options

NEXSYS Modules include three mounting options 1) In-Line Boot, 2) Bracket, and 3) Rail (M81714/5-5, M81714/16-5 Series Mounting Track, Type 1).

In-line Boot Mounting

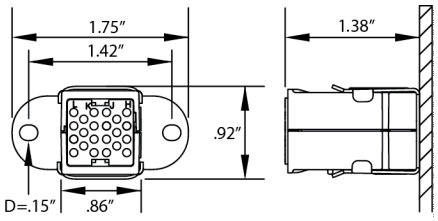
Figure 3.3.0.0-A



NEXSYS Modules shall use the In-Line Boot for harness mounting, and industry-standard methods shall be followed. The In-Line Boot is included with every NEXSYS Module and can be discarded if Bracket or Rail is used for mounting. Additional In-Line Boots may be ordered separately (P/N: 22-004).

Bracket Mounting

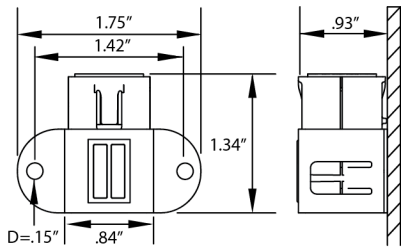
Figure 3.3.0.0-B



Right Angle Bracket: Mounts to a surface with fasteners (not included), with or without the NEXSYS Module installed. Insert the NEXSYS Module into the Right Angle Bracket until it has “clicked” securely into place. Removal of the NEXSYS Module from the Right Angle Bracket involves releasing side retaining clips. It is not necessary to remove the Right Angle Bracket from the mounting surface to release the NEXSYS Module. Bracket hole spacing is consistent with many standard relay mounting options.

Right angle brackets may be ordered with the NEXSYS Module or separately (P/N: 22-005).

Figure 3.3.0.0-C

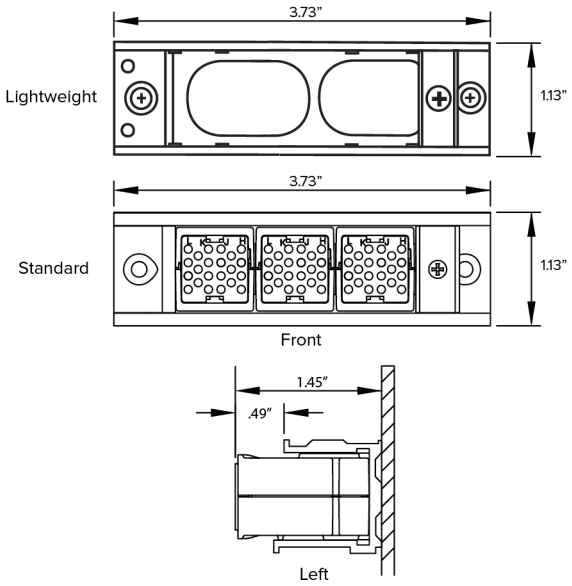


Flush Bracket: Mounts to a surface with fasteners (not included), and the NEXSYS Module is installed securely between the Flush Bracket mounting surface. Removal of the NEXSYS Module from the Flush Bracket involves removing the fasteners. Flush Bracket mounting-hole spacing is consistent with many standard relay mounting options.

Flush brackets may be ordered with the NEXSYS Module or separately (P/N: 22-011).

Rail Mounting

Figure 3.3.0.0-D



NEXSYS Modules mount into the Type 1 Rail (M81714/5-5, M81714/16-5) and secure into place, using the locking clamp included with the Rail. Each NEXSYS Modules requires two Rail positions. Removal of the NEXSYS Module from Rail involves releasing the locking clamp.

M81714 Series Mounting Track, Type 1 Rails with capacity for up to 3 NEXSYS Modules are available from Applied Avionics and may be ordered separately, Standard (P/N: 22-026).

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4.0 VIVISUN® Body Configurations

Summary Description

NEXSYS Component Technology can be packaged inside VIVISUN Compact or High Capacity bodies. NEXSYS components can be specified alone or in combination with electromechanical switches as shown in Section 4.1. Additional information on VIVISUN bodies, including dimensions and specific illuminated cap options, can be found in the VIVISUN Datasheet or Technical Guide.

VIVISUN Datasheet: https://www.appliedavionics.com/pdf/LED_R-2Brochure.pdf

VIVISUN Technical Guide

For additional VIVISUN switch body properties, reference the following data sheet:
https://www.appliedavionics.com/pdf/LED_R-2Brochure.pdf

4.1 Component Configurations

4.1.1 VIVISUN Compact Bodies

VIVISUN Compact Bodies can accommodate up to two Series A components in three specific component combinations. Only combinations utilizing at least one NEXSYS component are shown, see Figure 4.1.1.0-A.

Figure 4.1.1.0-A

	No Switch Poles A B	1 Switch Pole A B
Series A only components	SERIES A · OPEN - or - SERIES A · SERIES A	SWITCH · SERIES A

4.1.2 VIVISUN High Capacity Bodies

VIVISUN High Capacity bodies can accommodate 22 specific combinations of Series A, C, N and R component combinations based on the Series of components specified as shown below. Only combinations utilizing at least one NEXSYS component are shown, see Figure 4.1.2.0-A.

Figure 4.1.2.0-A

	No Switch Poles H J K L	1 Switch Pole H J K L	2 Switch Poles H J K L	3 Switch Pole H J K L
Series A only components	SERIES A · SERIES A · SERIES A · OPEN - or - SERIES A · SERIES A · SERIES A · SERIES A	SWITCH · SERIES A · SERIES A · OPEN - or - SWITCH · SERIES A · SERIES A · SERIES A	SWITCH · SERIES A · OPEN · SWITCH - or - SWITCH · SERIES A · SERIES A · SWITCH	SWITCH · SWITCH · SERIES A · SWITCH
Series C components	OPEN · SERIES C · OPEN - or - SERIES A · SERIES C · OPEN - or - SERIES A · SERIES C · SERIES A	SWITCH · SERIES C · OPEN - or - SWITCH · SERIES C · SERIES A	SWITCH · SERIES C · SWITCH	
Series N components	OPEN · SERIES N · OPEN - or - SERIES A · SERIES N · OPEN - or - SERIES A · SERIES N · SERIES A	SWITCH · SERIES N · OPEN - or - SWITCH · SERIES N · SERIES A	SWITCH · SERIES N · SWITCH	
Series R components	OPEN · SERIES R - or - SERIES A · SERIES R	SWITCH · SERIES R		

4.2 Termination

VIVISUN Compact bodies require a specially keyed solderless Connector Plug (P/N 18-442). Plugs can be ordered with VIVISUN Compact bodies or ordered separately. An Extraction Tool (P/N 18-234) is required to remove the Connector Plug from the VIVISUN Compact body. The Connector Plug can be inserted into the VIVISUN Compact body before or after installation. Please note, this connector plug is different than the plug required for switch/indicator bodies that do not contain any NEXSYS components.

Figure 4.2.0.0-A

Pins	Compact Body	Connector Plug
A-G	Illumination Circuits	 P/N 18-442
A1-A4, B1-B4	NEXSYS Component or switch Contacts	

Connector Plug designed to accept 20, 22, or 24 gauge wire terminated with MIL-C-39029/22-192 (P/N 18-219) crimp sockets. Wires with the sockets crimped on can be inserted into and extracted from the Connector Plug using a M81969/14-02 (P/N 18-216) extraction tool.

VIVISUN High Capacity bodies require a specially keyed solderless Connector Plug (P/N 18-440). Plugs can be ordered with VIVISUN High Capacity bodies or ordered separately. An Extraction Tool (P/N 18-234) is required to remove the Connector Plug from the VIVISUN High Capacity body. The Connector Plug can be inserted into the VIVISUN High Capacity body before or after installation. Please note, this connector plug is different than the plug required for switch/indicator bodies that do not contain any NEXSYS components.

Figure 4.2.0.0-B

Pins	High Capacity Body	Connector Plug
A-G	Illumination Circuits	 P/N 18-440
H1-H4, L1-L4, J1-J4, K1-K4	NEXSYS Component or switch Contacts	

Connector Plug designed to accept 20, 22, or 24 gauge wire terminated with MIL-C-39029/22-192 (P/N 18-219) crimp sockets. Wires with the sockets crimped on can be inserted into and extracted from the Connector Plug using a M81969/14-02 (P/N 18-216) extraction tool.

4.3 Installation

For VIVISUN body installation instructions, reference the VIVISUN Advanced Lighted Pushbutton Switches and Indicators section on the following web page: https://www.appliedavionics.com/installation-instructions.html

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5.0 NEXSYS® Thru-hole Devices

The following NEXSYS components are available as a stand-alone Thru-hole device. See NEXSYS® Components for a complete description of the functionality of each component. NEXSYS Components are categorized according to application function, and summarized in the table below.

Figure 5.0.0.0-A		
Function	**Description**	**Series**
Data Conversion		
ARINC 429 Signal Converters	Autonomous ARINC 429 receivers with the protocol logic necessary to capture and convert a specified data-word to discrete output(s), controlled by the decode of a single label and bit, multiple-bits, or multi-bit Binary Decode (BD), see 2.1.1	SERIES N SERIES R
Signal Switching/Control		
Defined Logic	Digital electronic device that performs Boolean logic gate operations AND, OR, NOT, NAND, NOR, XOR, XNOR, as well as BUFFER, see 2.2.1	SERIES C
Solid State Relay	Normally Open (NO) and Normally Closed (NC) solid-state relays available individually (SSR) or in a combination of four (SSRCH). The bidirectional inputs are polarity insensitive, and the device performs buffered switching with optical isolation between inputs and outputs, see 2.2.2	SERIES A SERIES C
State Control		
Electronic Latch	Electronic latching with multiple trigger modes to activate orthogonal switching (flip-flop) between two known states and a 1Hz blink output, see 2.3.1	SERIES C
Electronic Rotary	Electronic rotary control that performs incremental switching through a loop of up to four latched output states, controlled by input level transitions, see 2.3.2	SERIES C
Timing		
Pulse/Timer	Dual-channel edge detector and pulse generator with independent channels to perform stable retriggerable/resettable one-shot operation for fixed timing applications. Pulse-width output timing options range from 125 ms to 20 sec, see 2.4.1	SERIES C
Time Delay	Time-delay output, controlled by input triggers or power-up. Output timing options range from 125 ms to 4 hrs, see 2.4.2	SERIES A
Square Wave Oscillator	Oscillating output controlled by input triggers or power-up. Frequency (cycles/sec) and Period (sec/cycle) options range from 0.25 Hz (4 sec) to 500 Hz (0.002 sec), see 2.4.3	SERIES A
Sensing		
Voltage Sensor	Direct Current (DC) voltage sensor performs undervoltage and overvoltage detection to trigger the output. Sensed-voltage (VSD1) setpoint options range from +1 to 48 VDC, and sensed-low voltage (VSD2) setpoint options range from 50 mVDC to 1000 mVDC (+1 VDC), see 2.5.1	SERIES A
Current Sensor (DC)	Direct Current (DC), low-side current sensor that performs undercurrent and overcurrent detection to trigger the output. Sensed-current setpoint options range from 10 mA to 1000 mA (1.0 Amp), see 2.5.2	SERIES A
Passive		
Diode Pack	Package of two diodes specified as either commercial (1N6484) or military (1N5621JANTX) grade, see 2.6.1	SERIES A

5.1 Dimensions and Pin Spacing

Each Component Series (Series A, Series C, Series N, and Series R) has specific external component dimensions and pin spacing. All of the Thru-hole devices use a 0.025” diameter pin for thru-hole soldering.

Figure 5.1.0.0-A Series A

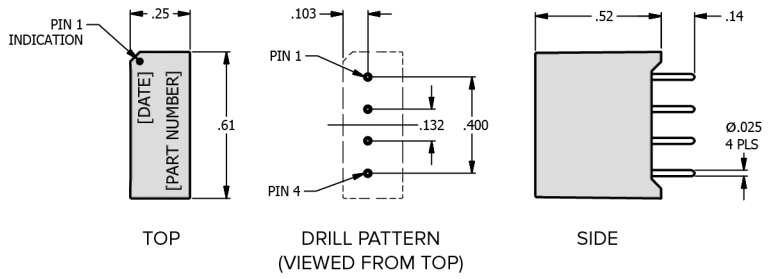


Figure 5.1.0.0-B Series C

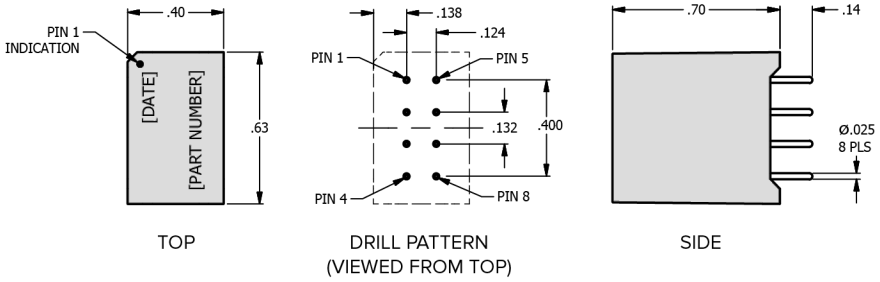


Figure 5.1.0.0-C Series N

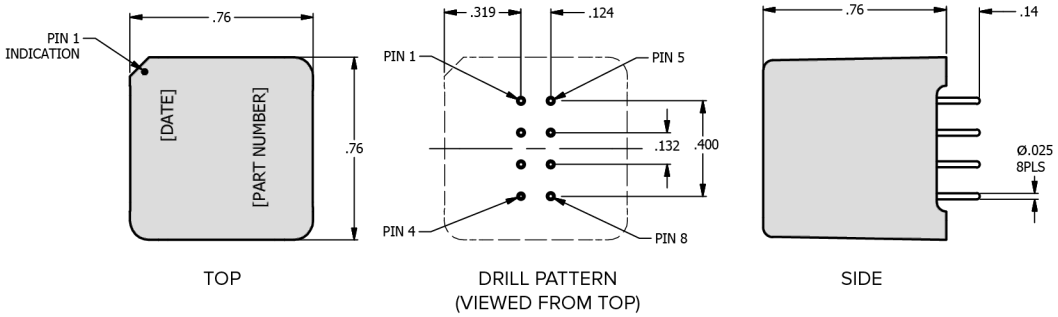
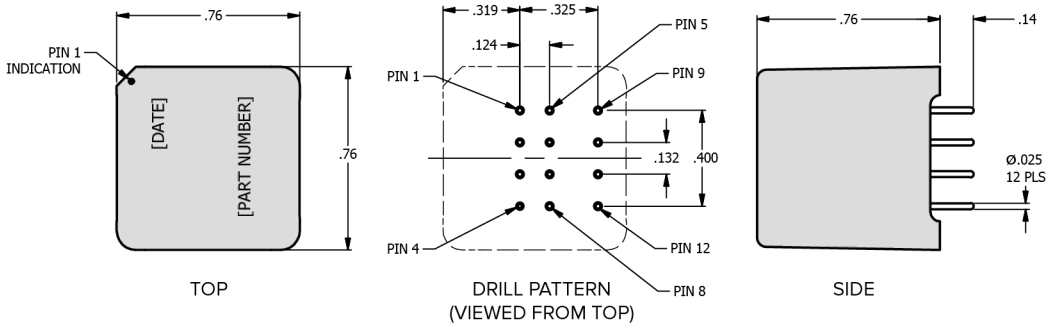


Figure 5.1.0.0-D Series R



Operating Parameters

Figure 5.1.0.0-E

Description	Parameters
Physical	
Weight	Series A: 3.0 grams (0.1 ounces) max. Series C: 4.5 grams (0.2 ounces) max. Series N: 8.5 grams (0.3 ounces) max. Series R: 8.5 grams (0.3 ounces) max.
Materials	Housing (Carbon Epoxy)
Environmental	
Temperature	Operating/Non-operating -55C to +85C
Altitude	-15,000 to +55,000 ft
Salt and Humidity	Humidity: 240 hrs, Salt: 96 hrs
Shock	20 G Sawtooth, 75 G half-sine
Vibration	10 to 2000 Hz 15 G
Electrical and Functional Performance	
See the Qualification Table (Appendix A) for electrical performance of each solderable component. Testing meets or exceeds the defined levels for RTCA/DO-160, MIL-STD-202 and MIL-STD-810.	

5.2 Installation

NEXSYS Thru-hole devices should be soldered to a rigid printed circuit board with thickness ranging from 0.062" - 0.093". Soldering on a flexible PCB is not recommended. Components are to be soldered to PCB per IPC J-STD-001G. The class used for soldering is per application requirements. Pins are thru-hole and not intended to be crimped. Lead-free soldering is not recommended for NEXSYS Thru-hole devices.

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6.0 Component Pinout

Component Series Pinout

Four Series designations, Series A, Series C, Series N, and Series R define the dimensions, packaging options and number of I/O of NEXSYS Components. Series A Pins are numbered 1-4, Series C and Series N are numbered 1-8 and Series R are numbered 1-12. The tables below correlate base pin numbers identified in each component section to the actual pin identification of each packaging form factor: NEXSYS Module, VIVISUN Body, and Thru-Hole Devices, see Figure 6.0.0.0-A – Figure 6.0.0.0-D.

The Part Configurator will prioritize the correct position of each component inside either a VIVISUN body or NEXSYS Module, and a pinout is provided at the time of part configuration. The pin identification is marked on the connector plug, except for Thru-Hole Devices since a connector is not used.

VIVISUN Compact Body

The VIVISUN Compact Body form factor, has two positions (Position A and B) and each position has the capacity to package one four-pin NEXSYS Component (i.e., Series A). The pin identification of VIVISUN Compact bodies is A1-A4 for Position A components and B1–B4 for Position B.

VIVISUN High-Capacity Body and NEXSYS Modules

The VIVISUN High-Capacity Body and NEXSYS Module form factor each have four positions (Position H, J, K and L), which afford the capacity to package a NEXSYS component of any Series. The pin identification of VIVISUN High-Capacity Bodies and NEXSYS Modules is H1–H4 for Position H, J1–J4 for Position J, K1–K4 for Position K, and L1–L4 for Position L. Series C, Series N, and Series R components are specified inside a VIVISUN High-Capacity Body (vs. Compact Body) due to the larger dimensions. Series A components occupy only one position, while Series C, Series N, and Series R occupy multiple positions. The VIVISUN High-Capacity Body affords packaging Series N or Series R components along with a Series A component, while the NEXSYS Module has capacity for, Series N or Series R components specified alone.

NEXSYS Thru-Hole Devices

The NEXSYS Thru-Hole Device form factor affords the use of stand-alone NEXSYS Components, primarily for Printed Circuit Board (PCB) applications. Thru-Hole pins are numbered 1-4, 1-8 or 1-12, matching the base pin numbers since there is no connector plug.

Series A Components

Figure 6.0.0.0-A

Base Pin ID	Pin ID when used in a VIVISUN Compact Body (See 4.1.1)	Pin ID when used in a VIVISUN High Capacity Body (See 4.1.2) or NEXSYS Module (See 3.1)	Pin ID when used as a Thru-Hole Device (See 5.1)
1	A1 or B1	H1 or J1 or K1 or L1	1
2	A2 or B2	H2 or J2 or K2 or L2	2
3	A3 or B3	H3 or J3 or K3 or L3	3
4	A4 or B4	H4 or J4 or K4 or L4	4

Series C Components

Figure 6.0.0.0-B			
Base Pin ID	Pin ID when One (1) Series C component is used in a VIVISUN High Capacity Body (See 4.1.2) or NEXSYS Module (See 3.1)	Pin ID when Two (2) Series C components are used in a NEXSYS Module (See 3.1)	Pin ID when used as a Thru-hole Device (See 5.1)
1	J1	H1 or K1	1
2	J2	H2 or K2	2
3	J3	H3 or K3	3
4	J4	H4 or K4	4
5	K1	J1 or L1	5
6	K2	J2 or L2	6
7	K3	J3 or L3	7
8	K4	J4 or L4	8

Series N Components

Figure 6.0.0.0-C		
Base Pin ID	Pin ID when used in a VIVISUN High Capacity Body (See 4.1.2) or NEXSYS Module (See 3.1)	Pin ID when used as a Thru-hole Device (See 5.1)
1	J1	1
2	J2	2
3	J3	3
4	J4	4
5	K1	5
6	K2	6
7	K3	7
8	K4	8

Series R Components

Figure 6.0.0.0-D		
Base Pin ID	Pin ID when used in a VIVISUN High Capacity Body (See 4.1.2) or NEXSYS Module (See 3.1)	Pin ID when used as a Thru-hole Device (See 5.1)
1	J1	1
2	J2	2
3	J3	3
4	J4	4
5	K1	5
6	K2	6
7	K3	7
8	K4	8
9	L1	9
10	L2	10
11	L3	11
12	L4	12

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Appendix A Qualification Tables

A.1 Environmental Qualifications

Figure A.1.1.0-A				
Test Description	Specification	Section	Category	Reference Levels
Altitude	RTCA/DO-160	4	A2, F2	-15,000, +55,000 Feet
	MIL-STD-202	105C	B	
	MIL-STD-810	500	Procedure II	
Temperature	RTCA/DO-160	4	F2	-55°C and +85°C
	MIL-STD-810	501/502	Procedure III	
Temperature Variation	RTCA/DO-160	5	S2	5 Cycles -55°C / +85°C
	MIL-STD-202	107	A	
	MIL-STD-810	503	1	
High Temperature Survival (Non-Operating)	MIL-STD-202	108A	A	+85°C, 96 Hours (Switch) +125°C, 96 Hours (NEXSYS Modules)
Humidity	RTCA/DO-160	6	B	240 Hours, +38°C / 65°C, > 90% RH 240 Hours, -10°C / 65°C, > 90% RH
	MIL-STD-202	106	N/A	
Operational Shock and Crash Safety	RTCA/DO-160	7	B	20 G Sawtooth
	MIL-STD-202	213	B	20G Acceleration, 75 G Half-Sine
	MIL-STD-810	516	N/A	N/A
Acceleration	RTCA/DO-160	7	B	20 G, 3 Axis
	MIL-STD-202	212	A	
	MIL-STD-810	513	Procedure III	
Vibration	RTCA/DO-160	8	R, U	10 to 2000 Hz, Sine on Random
	MIL-STD-202	204	B	10 to 2000 Hz 15 G
Explosive Atmosphere	RTCA/DO-160	9	E	N/A
	MIL-STD-202	109C	B	
Waterproofness	RTCA/DO-160	10	R	450 Litres / Hour 15 Gallons / Minute
	MIL-PRF-22885	4.7.20	Splash-proof	-10°C /+ 40°C 85% RH
Sand and Dust	RTCA/DO-160	12	D	Silica Media
	MIL-STD-202	110	N/A	
Fungus Resistance	RTCA/DO-160	13	F	Compliance by Material Selection
	MIL-PRF-22885	3.5.2	N/A	
Salt Fog	RTCA/DO-160	14	T	96 Hour Tests
	MIL-STD-202	101	A	

A.2 Electrical Qualifications

Figure A.1.2.0-A				
Test Description	Specification	Section	Category	Reference Levels
Power Input Aircraft Power	RTCA/DO-160	16.6; except as noted below	A and B	200ms / 50ms dropout (CS, CT, DL, ER, PT, SR429/4, TD, VS)**
		16.6.1.3 (Momentary Power Interrupt)	A and B	
			B	50ms dropout (EL, SR429/1, TD)**
			N/A	No digital circuitry. (SSR, TB, DP)**
		16.6.1.5, 16.6.2.2	B	Tests not applicable to Category A
		16.6.2.3	A	12V +/- 0.24V for 7 sec.
		16.6.2.4	A	37.8V -0/+2V for 1 sec.
	MIL-HDBK-704-8	LDC (102, 301, 401, 501, 602)	N/A	N/A
Spike / Transient	RTCA/DO-160	17	A	Power 600V, 10µsec, 50 ohms
Audio Frequency Conducted Susceptibility	RTCA/DO-160	18	Z	Power Input, 4V P to P, 1 to 150KHz
	MIL-STD-461	CS101	Curve 2	
Induced Signal Susceptibility	RTCA/DO-160	19	CW	10,000V/m, 120A/m, 350 and 800Hz
RF Conducted Susceptibility*	RTCA/DO-160	20	Y	300mA, 10KHz to 400MHz
	MIL-STD-461	CS114	Curve 5	109dBµA, 10KHz to 200MHz
	RTCA/DO-160	20	W	SSR3: 100mA, 10KHz to 400Hz
	MIL-STD-461	CS114	Curve 4	SSR3: 10KHz to 400Hz
RF Radiated Susceptibility*	RTCA/DO-160	20	Y	200V/m 2MHz to 18GHz
	MIL-STD-461	RS103	200V/m	
Conducted RF Emissions	RTCA/DO-160	21	P	150KHz to 152MHz
	MIL-STD-461	CE102	N/A	10KHz to 10MHz
Radiated RF Emissions	RTCA/DO-160	21	P	100MHz to 6GHz
	MIL-STD-461	RE102	N/A	10KHz to 6GHz
Lightning Induced Transient*	RTCA/DO-160	22	XXK3L3	Waveform 3, 600V, 1MHz, 10MHz, Single, Multiple, Burst Waveform 4, 300V, 69µsec Waveform 5A, 300V, 120µsec
	MIL-STD-461	CS117	L1	
Military Transient*	MIL-STD-461	CS115	N/A	5A 30nS 30/Sec for 1 minute
	MIL-STD-461	CS116	N/A	Damped Sinusoidal, 10KHz to 100MHz
Dielectric Withstanding	MIL-STD-202	301		1000 VAC
Electrostatic Discharge	RTCA/DO-160	25	A	15,000V, 150pF, 330 ohms
	MIL-STD-461	CS118	Level 4	
Magnetic Effect	RTCA/DO-160	15	Z	1° Deflection, at < 0.3m

** Stated EMC performance based on tests performed on an individually monitored component using unshielded cables as defined by the applicable EMC test document. The EMC performance of an installed system using NEXSYS components can be dependent on the actual installation environment and interconnection method.*

*** Key to Abbreviations Above: CS=Current Sensor, CT=Square Wave Oscillator, DL=Defined Logic, DP=Diode Pack, EL=Electronic Latch, ER=Electronic Rotary, PT=Pulse/Timer, SR429/1=ARINC 429 Signal Converter (/1M), SR429/4=ARINC 429 Signal Converter (/4M and /4D), SSR=Solid State Relay, TB=Terminal Block, TD=Time Delay, VS=Voltage Sensor*